

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	TOP LAYER 1		1.20mil		
	Dielectric 1	FR-4	8.00mil	4.5	
2	GND LAYER 2		1.20mil		
	Dielectric2	FR-4	8.00mil	4.5	
3	SIG H LAYER 3		1.20mil		
	Dielectric3	FR-4	8.00mil	4.5	
4	SIG V LAYER 4		1.20mil		
	Dielectric4	FR-4	8.00mil	4.5	
5	POWER LAYER 5		1.20mil		
	Dielectric5	FR-4	8.00mil	4.5	
6	BOTTOM LAYER 6		1.20mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				

- NOTES:
1. MATERIAL:  
NEIRA FR4 UL94V-0 COPPER CLAD BOTH SIDES.  
FINISHED COPPER WEIGHT INNER LAYERS (2 THRU 5) TO BE 3 OZ MINIMUM.  
FINISHED COPPER WEIGHT OUTER LAYERS (1 AND 6) TO BE 3 OZ MINIMUM.  
TOTAL PCB FINISHED THICKNESS TO BE 0.062 +/- 0.007.
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  3. FOR BOARD CONSTRUCTION SEE PCB STACK UP DETAIL.
  4. FINISHED LINE WIDTH TO BE +/- 20% OF GERBER DATA 1/1 FILES  
MINIMUM LINE 0.008 . MINIMUM SPACE 0.008
  5. HOLE DIAMETER SHALL BE FINISHED SOLDER-PLATED SIZE.  
HOLES TO BE PLATED THRU .001 MINIMUM COPPER.
  6. MINIMUM ANNULAR RING REQUIREMENT IS 0.002 FOR INTERNAL AND EXTERNAL LAYERS.
  7. NON-FUNCTIONAL PADS MAY BE REMOVED ON INNER LAYERS.
  8. CONSTRUCTION TO BE SOLDERMASK OVER BARE COPPER (SPOBC), USING LIQUID PHOTO-IMAGEABLE (LPI) COLOR GREEN. SOLDERMASK TO MEET QUALIFICATIONS OF IPC-S1-B40.
  9. SILKSCREEN USE WHITE NON-CONDUCTIVE INK. ALL COMPONENT AND TESTPOINT LANDS ARE TO BE FREE OF INK.
  10. MANUFACTURER SHALL PLACE THEIR UL LOGO, FLAME CODE UL94V-0 AND DATE CODE, ETCHED ON LAYER 6 (BOTTOM SIDE OF BOARD).
  11. HOT AIR SOLDER LEVELING (HASL), COVERAGE AND SOLDERABILITY SHALL MEET ANSI J-STD-003.
  12. BOARDS SHALL BE ACCEPTABLE AND REJECTABLE PER IPC-A-600 CLASS 2.
  13. BARE BOARDS SHALL BE 100% ELECTRICAL TESTED FOR RESISTANCE AND CONTINUITY AT 100 VOLTS MINIMUM, USING GERBER GENERATED NET LIST DATA.
  14. THE MARKING OF THE ELECTRICAL TESTING HOUSE SHALL BE PLACED ON THE BOARD USING A NONCONDUCTIVE EPOXY INK ON EITHER SIDE OF THE BOARD.
  15. COPPER THEIVING OF THE SIGNAL LAYERS IS NOT ALLOWED.

Symbol	Count	Hole Size	Plated	Hole Type	Uia/Pad	Hole Tolerance (+)	Hole Tolerance (-)
⊙	1862	15.00mil (0.381mm)	PTH	Round	Uia		
▽	5	40.00mil (1.016mm)	PTH	Round	Pad	0.00mil (0.000mm)	0.00mil (0.000mm)
⌘	62	42.00mil (1.067mm)	PTH	Round	Pad		
⊘	64	42.00mil (1.067mm)	PTH	Round	Pad	0.00mil (0.000mm)	0.00mil (0.000mm)
⊛	5	55.00mil (1.397mm)	PTH	Round	Pad	0.00mil (0.000mm)	0.00mil (0.000mm)
C	50	58.00mil (1.473mm)	PTH	Round	Pad		
○	4	75.00mil (1.905mm)	PTH	Round	Pad	0.00mil (0.000mm)	0.00mil (0.000mm)
◊	4	78.00mil (1.981mm)	NPTH	Round	Pad	0.00mil (0.000mm)	0.00mil (0.000mm)
⊞	35	86.00mil (2.184mm)	PTH	Round	Pad	0.00mil (0.000mm)	0.00mil (0.000mm)
◇	12	110.00mil (2.794mm)	PTH	Round	Pad		
B	4	118.00mil (2.997mm)	PTH	Round	Pad		
A	4	128.00mil (3.251mm)	NPTH	Round	Pad		
⌘	2	128.00mil (3.251mm)	NPTH	Slot	Pad	0.00mil (0.000mm)	0.00mil (0.000mm)
⌘	12	150.00mil (3.810mm)	NPTH	Round	Pad		
	2125 Total						

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.  
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

Q25010-PCB\_revT.PcbDoc  
DRILL DRAWING

