

Symbol	Count	Hole Size	Plated	Hole Tolerance (+)	Hole Tolerance (-)
✕	25	8.00mil	PTH	3.00mil	8.00mil
⊙	25	11.90mil	PTH	3.00mil	11.90mil
⊞	236	12.00mil	PTH	3.00mil	12.00mil
□	73	15.00mil	PTH		
⊖	2	24.00mil	NPTH		
▽	40	32.00mil	PTH		
✳	2	35.00mil	NPTH		
◇	1	39.00mil	NPTH		
▼	2	40.00mil	PTH		
✳	8	59.00mil	PTH	3.00mil	3.00mil
⊞	4	93.00mil	NPTH		
○	4	128.00mil	PTH		
	422 Total				

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.50mil	3.8	
1	Top Layer 1		1.40mil		
	Dielectric 1		5.60mil	4.2	
2	Layer 2 (GND)		0.70mil		
	Dielectric 4		20.00mil	4.2	
3	Layer 3 (U)		0.70mil		
	Dielectric 2		5.60mil	4.2	
4	Layer 4 (H)		0.70mil		
	Dielectric 5		20.00mil	4.2	
5	Layer 5 (PWR)		0.70mil		
	Dielectric 3		5.60mil	4.2	
6	Bottom Layer 6		1.40mil		
	Bottom Solder	Solder Resist	0.50mil	3.8	
	Bottom Overlay				

## FABRICATION NOTES:

- MATERIAL SELECTION:  
370HR OR EQUIVALENT UL RECOGNIZED ZPMV2 MIN. 130C FLAME CLASS V-0 OR BETTER,  
MINIMUM CTI RATING OF 175, 0.062 +/- 0.007 THICK. MATERIAL PER IPC-4101  
SOLDERABLE SURFACES TO BE ENIG (ELECTROLESS NICKEL IMMERSION GOLD) FINISH.  
STARTING COPPER WEIGHT INTERNAL 1/2 oz. MINIMUM  
STARTING COPPER WEIGHT EXTERNAL 1/2 oz. MINIMUM
- SOLDER RESIST: THE USE OF SOLDER RESIST COATING SHALL BE IN ACCORDANCE WITH THE REQUIREMENTS OF IPC-SM-840. ALL SOLDERABLE SURFACES ARE TO BE FREE OF SOLDER RESIST. COLOR - GREEN. USE LIQUID PHOTOIMAGEABLE RESIST. MATTE FINISH.
- SILKSCREEN: USE WHITE NON-CONDUCTIVE INK. ALL COMPONENT AND TESTPOINT LANDS ARE TO BE FREE OF INK. PLACE UL 94V-0 RATING ON SOLDER SIDE IN SILKSCREEN ONLY.
- MANUFACTURER'S IDENTIFICATION: ADD IN ETCH OR TO SILKSCREEN.
- ELECTRICAL BARE BOARD TEST REQUIRED.
- DRILL SIZES ARE FINISHED SIZES AFTER PLATING.
- FABRICATE TO MEET EU RoHS DIRECTIVE.
- PCB MUST HAVE UL 94V-0 AND CTI RATING MARKED ON ONE SIDE.
- MAX WARP AND TWIST NOT TO EXCEED 0.010 PER LINEAR INCH.
- MIN ANNULAR RING: 0.003. MIN PLATED HOLE WALL THICKNESS 0.001.
- DIMENSIONAL TOL: XX +/- 0.010. XXX +/- 0.005.
- FABRICATE IN ACCORDANCE WITH IPC-600 OR IPC-6012 LATEST REVISION. CLASS 2.
- COPPER THEIVING OF THE SIGNAL LAYERS IS NOT ALLOWED.
- PCB FABRICATOR IS ALLOWED TO ADJUST PARAMETERS TO ACHIEVE REQUIRED TRACE IMPEDANCE +/-10%.

## IMPEDANCE REQUIREMENTS:

LAYER	WIDTH	SPACING	REQUIRED IMPEDANCE
1	8.2mil	7mil	90 OHMS DIFFERENTIAL
6	8.2mil	7mil	90 OHMS DIFFERENTIAL

