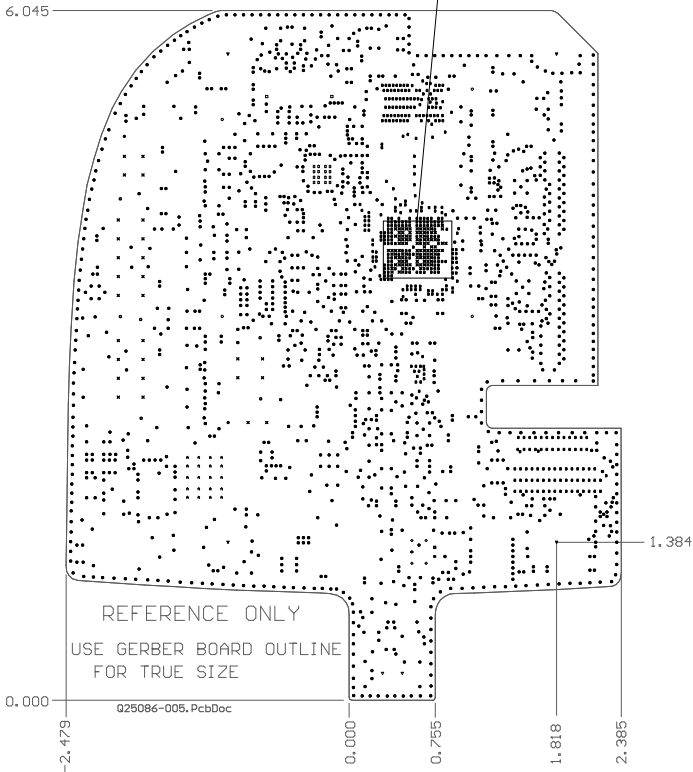


FABRICATION NOTES:

1. MATERIAL SELECTION:
370HR OR EQUIVALENT UL RECOGNIZED ZPMV2 MIN. 130C FLAME CLASS V-0 OR BETTER,
MINIMUM CTI RATING OF 175, .062 +/- 0.007 THICK. MATERIAL PER IPC-6101
SOLDERABLE SURFACES TO BE ENIG (ELECTROLESS NICKEL IMMERSION GOLD) FINISH.
STARTING COPPER WEIGHT INTERNAL 1/2 oz. MINIMUM
STARTING COPPER WEIGHT EXTERNAL 1/3 oz. MINIMUM
2. SOLDER RESIST: THE USE OF SOLDER RESIST COATING SHALL BE IN
ACCORDANCE WITH THE REQUIREMENTS OF IPC-SM-840. ALL SOLDERABLE
SURFACES ARE TO BE FREE OF SOLDER RESIST. COLOR - GREEN.
USE LIQUID PHOTOMAGEABLE RESIST, MATTIE FINISH.
3. SILKSCREEN: USE WHITE NON-CONDUCTIVE INK. ALL COMPONENT AND
TESTPOINT LANDS ARE TO BE FREE OF INK.
PLACE UL 94V-0 RATING ON SOLDER SIDE IN SILKSCREEN ONLY.
4. MANUFACTURER'S IDENTIFICATION: ADD IN ETCH OR TO SILKSCREEN.
5. ELECTRICAL BARE BOARD TEST REQUIRED.
6. DRILL SIZES ARE FINISHED SIZES AFTER PLATING.

7. FABRICATE TO MEET EU RoHS DIRECTIVE.
8. PCB MUST HAVE UL 94V-0 AND CTI RATING MARKED ON ONE SIDE.
9. MAX WARP AND TWIST NOT TO EXCEED 0.010 PER LINEAR INCH.
10. MIN ANNULAR RING: 0.003. MIN PLATED HOLE WALL THICKNESS 0.001.
11. DIMENSIONAL TOL: XX +/- 0.010. XXX +/- 0.005.
12. FABRICATE IN ACCORDANCE WITH IPC-600 OR IPC-6012 LATEST REVISION. CLASS 2.
13. COPPER THEIVING OF THE SIGNAL LAYERS IS NOT ALLOWED.
14. PCB FABRICATOR IS ALLOWED TO ADJUST PARAMETERS TO ACHIEVE REQUIRED TRACE IMPEDANCE +/-10%.
15. ALL .0079 DIAMETER HOLES ARE VIPPO VIAS



Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.8	
1	Top Layer 1		1.40mil		
	Dielectric 1	FR-4	3.80mil	4.2	
2	Layer 2 (GND)		0.60mil		
	Dielectric 2		5.00mil	4.2	
3	Layer 3 (Sig HS-U)		0.60mil		
	Dielectric 3		8.00mil	4.2	
4	Layer 4 (Sig H)		0.60mil		
	Dielectric 4		5.00mil	4.2	
5	Layer 5 (Power +5V)		0.60mil		
	Dielectric 5		10.00mil	4.2	
6	Layer 6 (Power +3V)		0.60mil		
	Dielectric 6		5.00mil	4.2	
7	Layer 7 (Sig H)		0.60mil		
	Dielectric 7		8.00mil	4.2	
8	Layer 8 (Sig HS-U)		0.60mil		
	Dielectric 8		5.00mil	4.2	
9	Layer 9 (GND)		0.60mil		
	Dielectric 9		3.80mil	4.2	
10	Bottom Layer 10		1.40mil		
	Bottom Solder	Solder Resist	0.40mil	3.8	
	Bottom Overlay				

Symbol	Count	Hole Size	Plated	Hole Type	Via/Pad	Hole Tolerance (+)	Hole Tolerance (-)
⌘	99	7.90mil (0.201mm)	PTH	Round	Via	3.00mil (0.076mm)	7.90mil (0.201mm)
D	16	7.95mil (0.202mm)	PTH	Round	Via	3.00mil (0.076mm)	7.95mil (0.202mm)
B	400	8.00mil (0.203mm)	PTH	Round	Via	3.00mil (0.076mm)	8.00mil (0.203mm)
A	20	11.90mil (0.302mm)	PTH	Round	Via	3.00mil (0.076mm)	11.90mil (0.302mm)
⊙	1587	12.00mil (0.305mm)	PTH	Round	Via	3.00mil (0.076mm)	12.00mil (0.305mm)
□	2	24.00mil (0.610mm)	PTH	Round	Pad		
▽	2	35.00mil (0.889mm)	NPTH	Round	Pad		
⊠	1	39.00mil (0.991mm)	NPTH	Round	Pad		
⊛	2	40.00mil (1.016mm)	PTH	Round	Pad		
⌘	28	55.00mil (1.397mm)	PTH	Round	Pad		
◇	4	93.00mil (2.362mm)	NPTH	Round	Pad		
⊙	6	118.00mil (2.997mm)	NPTH	Round	Pad		
⊙	2	125.00mil (3.175mm)	NPTH	Round	Pad		
⊙	4	166.14mil (4.220mm)	PTH	Round	Pad		
▽	4	221.00mil (5.613mm)	NPTH	Round	Pad		
2127 Total							

Impedance requirements: PCB trace widths and spacings

	100 ohm diff	100(Trace Spacing)	90 ohm diff	90(Trace Spacing)	50 ohm
Layer 1			0.0055	0.0075	0.0055
Layer 2 (Gnd Plane)					
Layer 3	0.005	0.008			0.006
Layer 4					
Layer 5 (Power Plane)					
Layer 6 (Power Plane)					
Layer 7	0.005	0.008			
Layer 8	0.005	0.008			0.006
Layer 9 (Gnd Plane)					
Layer 10					