Saturn Series

TBR3206 Machine Controller

1259197 / 1273393

Functional Circuit Test

Revision D

Revision	Changes	Engineer	Date
A	Initial	RDH	2023-11-28
B	Added software commands + updated most sections	RDH	2024-04-01
C	Updated pass criteria to fit software changes + note on test sequencing + removed current and clipped pulse checks	RDH	2025-01-09
D	Updated tolerance window for nominal current tests	RDH	2025-03-04

Table of Contents:

Setup:

This test procedure is to be executed on the 1259197 or 1273393 PCBA. The serial port used for this test is inaccessible after the cover is assembled onto the board as part of the 1260556 or 1273390 assembly.

Commands used for this test procedure will be sent and received over the UART debug port (J7). This UART communication uses 115200 baud, 8 data bits, 1 stop bit. This UART uses 3.3V TTL logic levels. This UART port can be accessed with TX on J7-3, RX on J7-4, and GND on J7-5.

1. Install PCBA in test fixture before assembly of top case.
2. Apply +36V to J8 and J28-33. Apply COM to J9. Note that there is a high amount of inrush current when this board is powered. The power supply should be capable of supplying 70A.

Note on Test Sequence Ordering:

In the interest of reducing total test time and number of power cycles required to complete this test procedure:

> At the discretion of the test operator, the tests described after Setup can be completed in any order unless otherwise specified.

On the high-power outputs of the 1259197 / 1273393 PCBA (Half Bridges, H-Bridges, LSDs), each fault only disables further use of that specific driver until the fault is cleared by a power cycle. A fault on one driver does not prevent the use of another.

For example, if the open load test is performed on Half Bridge 1 which results in an open load fault, the open load test for Half Bridge **2** could be performed before power cycling to clear the fault on Half Bridge 1, and likewise for Half Bridge 3 and the H-Bridges and the LSDs.

All power cycles in this test procedure are marked (optional) to allow for this sequencing.

Revision Verification:

1. Send command `'version'` to read the hardware and software versions.
2. Output shall include the following lines which match version numbers on the drawing

Example:
Scrub Controller Module
FCT SW Rev:01.12.00.1
HW Rev: 3.00
FPGA Module
SW_Rev:01.12.00.04

SPI Flash:

1. Send command ‘flash e’ to erase FCT flash sector.
2. Send command ‘flash w’ to write test data to FCT flash sector.
3. Confirm response of “Flash write operation successful”
4. Send command ‘flash r’ to read back test data.
5. Confirm response of “Flash read and validation successful”

EEPROM :

1. Write to EEPROM with ‘eeprom w=499’
2. Power cycle board.
3. Read from EEPROM with ‘eeprom r’
4. Response shall include ‘499’

CAN:

1. Connect a CAN interface to CAN-H at J28-28 and CAN-L J28-29
2. Configure the CAN bus to operate at 125kb/s
3. Confirm receipt of message ID 0x702 at CAN node 0x02
4. Value of message shall be 0x7F

Note: Previous procedure included transmitting a message, this is no longer required.

Power Supplies and Voltage Regulators:

1. Measure 5V regulator by measuring TP58
2. TP58 shall be 5V ± 5%.
3. Measure 3.3V regulator by measuring TP47
4. TP47 shall be 3.3V ± 5%.
5. Measure 12V regulator by measuring TP44
6. TP44 shall be 12V ± 5%.
7. Measure the current limited 5V supply by measuring J27-33
8. J27-33 shall be 5V ± 5%.
9. Apply a 200Ω 1W load between J27-33 and COM
10. J27-33 shall be 1.7V ± 10%
11. Remove load from J27-33.
12. Apply a 200Ω 1W load between J28-12 and COM
13. Enable the limited 12V supply with the command ‘12v e=1’
14. Measure the limited 12V supply by measuring J28-12

15. J28-12 shall be 12V ± 10%
16. Disable the limited 12V supply with the command ‘12v e=0’
17. J28-12 shall be 0V
18. Remove load from J28-12

Hour Meter:

1. Measure J27-24 with respect to COM
2. J27-24 shall be 0V ± 0.2V
3. Enable hour meter output with ‘hour e=1’
4. Measure J27-24
5. J27-24 shall be 5V ± 5%
6. Disable hour meter output with ‘hour e=0’
7. Measure J27-24
8. J27-24 shall be 0V ± 0.2V

Analog Inputs:

Power Source 1:

1. Read power source 1 input with ‘Power_Source ?’
2. Power source 1 value shall be 0V and undervoltage shall be true.
3. Apply 36V to J28-34
4. Read power source 1 input with ‘Power_Source ?’
5. Power source 1 value shall be 36V± 5% and undervoltage shall be false.
6. Reduce voltage on J28-34 from 36V to 15V
7. Read power source 1 undervoltage with ‘Power_Source ?’
8. Power source 1 undervoltage value shall be true.
9. Remove bias from J28-34

Power Source 2:

1. Note that Power Source 2 must be high for the test software to operate.
2. Read power source 2 input with ‘Power_Source ?’
3. Power source 2 value shall be 36V± 5% and undervoltage shall be false.

Power Source 3:

1. Read power source 3 input with ‘Power_Source ?’
2. Power source 3 value shall be 0V and undervoltage shall be true.
3. Apply 36V to J28-25
4. Read power source 3 input with ‘Power_Source ?’
5. Power source 3 value shall be 36V± 5% and undervoltage shall be false.

6. Reduce voltage on J28-25 from 36V to 15V
7. Read power source 3 undervoltage with ‘Power_Source ?’
8. Power source 3 undervoltage value shall be true.
9. Remove bias from J28-25

5V Input 1:

1. Read 5V Input 1 voltage with ‘5vin ?’
2. 5V Input 1 voltage shall be 0V
3. Apply 5V to J27-25
4. Read 5V Input 1 voltage with ‘5vin ?’
5. 5V Input 1 voltage shall be 5V ± 5%
6. Remove bias from J27-25

5V Input 2:

1. Read 5V Input 2 voltage with ‘5vin ?’
2. 5V Input 2 voltage shall be 0V
3. Apply 5V to J27-34
4. Read 5V Input 1 voltage with ‘5vin ?’
5. 5V Input 2 voltage shall be 5V ± 5%
6. Remove bias from J27-34

5V Input 3:

1. Read 5V Input 3 voltage with ‘5vin ?’
2. 5V Input 3 voltage shall be 0V
3. Apply 5V to J28-20
4. Read 5V Input 3 voltage with ‘5vin ?’
5. 5V Input 3 voltage shall be 5V ± 5%
6. Remove bias from J28-20

Digital Inputs:

1. Read SW1 with ‘inputs ?’
2. SW1 shall be false.
3. Apply 36V to J27-18
4. Read SW1 with ‘inputs ?’
5. SW1 shall be true.
6. Remove bias from J27-18

7. Read SW2 with ‘inputs ?’
8. SW2 shall be false.
9. Apply 36V to J27-19

10. Read SW2 with ‘inputs ?’
11. SW2 shall be true.
12. Remove bias from J27-19

13. Read SW3 with ‘inputs ?’
14. SW3 shall be false.
15. Apply 36V to J27-26
16. Read SW3 with ‘inputs ?’
17. SW3 shall be true.
18. Remove bias from J27-26

19. Read SW4 with ‘inputs ?’
20. SW4 shall be false.
21. Apply 36V to J27-27
22. Read SW4 with ‘inputs ?’
23. SW4 shall be true.
24. Remove bias from J27-27

25. Read nSW1 with ‘inputs ?’
26. nSW1 shall be false.
27. Apply 0V to J27-11
28. Read nSW1 with ‘inputs ?’
29. nSW1 shall be true.
30. Remove bias from J27-11

31. Read nSW2 with ‘inputs ?’
32. nSW2 shall be false.
33. Apply 0V to J27-28
34. Read nSW2 with ‘inputs ?’
35. nSW2 shall be true.
36. Remove bias from J27-28

37. Read nSW3 with ‘inputs ?’
38. nSW3 shall be false.
39. Apply 0V to J27-29
40. Read nSW3 with ‘inputs ?’
41. nSW3 shall be true.
42. Remove bias from J27-29

43. Read nSW4 with ‘inputs ?’
44. nSW4 shall be false.

45. Apply 0V to J27-31
46. Read nSW4 with `'inputs ?'`
47. nSW4 shall be true.
48. Remove bias from J27-31

49. Read nSW5 with `'inputs ?'`
50. nSW5 shall be false.
51. Apply 0V to J27-23
52. Read nSW5 with `inputs ?`
53. nSW5 shall be true.
54. Remove bias from J27-23

55. Read nSW6 with `'inputs ?'`
56. nSW6 shall be false.
57. Apply 0V to J27-30
58. Read nSW6 with `'inputs ?'`
59. nSW6 shall be true.
60. Remove bias from J27-30

61. Read nSW7 with `'inputs ?'`
62. nSW7 shall be false.
63. Apply 0V to J27-22
64. Read nSW7 with `'inputs ?'`
65. nSW7 shall be true.
66. Remove bias from J27-22

67. Read nSW8 with `'inputs ?'`
68. nSW8 shall be false.
69. Apply 0V to J27-32
70. Read nSW8 with `'inputs ?'`
71. nSW8 shall be true.
72. Remove bias from J27-32

73. Read nSW9 with `'inputs ?'`
74. nSW9 shall be false.
75. Apply 0V to J27-21
76. Read nSW9 with `'inputs ?'`
77. nSW9 shall be true.
78. Remove bias from J27-21

79. Read nSW10 with `'inputs ?'`

80. nSW10 shall be false.
81. Apply 0V to J27-20
82. Read nSW10 with `'inputs ?'`
83. nSW10 shall be true.
84. Remove bias from J27-20

Half Bridges:

Half Bridge 1:

Open Load Test:

1. Enable Half Bridge 1 at 50% duty cycle with `'hb1 v=1800'`
2. Read open fault with `'hb1 ?'`
3. (optional) Power cycle to clear faults

Nominal Load Test:

1. Apply a 10Ω 150W load between J16 and J17
2. Enable Half Bridge 1 at 50% duty cycle with `'hb1 v=1800'`
3. Read Half Bridge 1 current with `'hb1 ?'`
4. Half Bridge 1 current shall be 3.6A ± 1A
5. Disable Half Bridge 1 with `'hb1 v=0'`
6. Remove the 10Ω load between J16 and J17

Overcurrent Test:

1. Apply a 0.5Ω 2kW load between J16 and J17
2. Enable Half Bridge 1 at 50% duty cycle with `'hb1 v=1800'`
3. Read Half Bridge 1 status with `'hb1 ?'`
4. Half Bridge 1 Fault shall display “Current Limit” or “Shorted Load”
5. (optional) Power cycle to clear faults
6. Remove load from J16 and J17

Half Bridge 2:

Open Load Test:

1. Enable Half Bridge 1 at 50% duty cycle with `'hb2 v=1800'`
2. Read open fault with `'hb2 ?'`
3. (optional) Power cycle to clear fault

Nominal Load Test:

1. Apply a 10Ω 150W load between J14 and J15
2. Enable Half Bridge 2 at 50% duty cycle with `'hb2 v=1800'`

3. Read Half Bridge 2 current with ‘hb2 ?’
4. Half Bridge 2 current shall be 3.6A ± 1A
5. Disable Half Bridge 2 with ‘hb2 v=0’
6. Remove the 10Ω load between J15 and J15

Overcurrent Test:

1. Apply a 0.5Ω 2kW load between J14 and J15
2. Enable Half Bridge 2 at 50% duty cycle with ‘hb2 v=1800’
3. Read Half Bridge 2 status with ‘hb2 ?’
4. Half Bridge 2 Fault shall display "Current Limit” or “Shorted Load”.
5. (optional) Power cycle to clear fault
6. Remove load from J14 and J15

Half Bridge 3:

Open Load Test:

1. Enable Half Bridge 3 at 50% duty cycle with ‘hb3 v=1800’
2. Read open fault with ‘hb3 ?’
3. (optional) Power cycle to clear fault

Nominal Load Test:

1. Apply a 10Ω 150W load between J12 and J13
2. Enable Half Bridge 3 at 50% duty cycle with ‘hb3 v=1800’
3. Read Half Bridge 3 current with ‘hb3 ?’
4. Half Bridge 3 current shall be 3.6A ± 1A
5. Disable Half Bridge 3 with ‘hb3 v=0’
6. Remove the 10Ω load

Overcurrent Test:

1. Apply a 0.5Ω 2kW load between J12 and J13
2. Enable Half Bridge 3 at 50% duty cycle with ‘hb3 v=1800’
3. Read Half Bridge 3 status with ‘hb3 ?’
4. Half Bridge 3 Fault shall display “Current Limit” or “Shorted Load”
5. (optional) Power cycle to clear fault
6. Remove load from J12 and J13

H-Bridges:

H-Bridge 1:

Open Load Test:

1. Enable H-Bridge 1 at 50% duty cycle with `'fb1 e=500'`
2. Read open fault with `'fb1 ?'`
3. (optional) Power cycle to clear fault

Nominal Load Test:

1. Apply a 10Ω 150W load between J28-4 and J28-2
2. Enable H-Bridge 1 at 50% duty cycle FORWARD with `'fb1 e=500'`
3. Read H-Bridge 1 current with `'fb1 ?'`
4. H-Bridge 1 current shall be 3.6A ± 0.5A
5. Disable H-Bridge 1 with `'fb1 e=0'`
6. Enable H-Bridge 1 at 50% duty cycle REVERSE with `'fb1 r=500'`
7. Read H-Bridge 1 current with `'fb1 ?'`
8. H-Bridge 1 current shall be 3.6A ± 0.5A
9. Disable H-Bridge 1 with `'fb1 r=0'`
10. Remove the 10Ω load between J28-4 and J28-2

Overcurrent Test:

1. Apply a 1.5Ω 600W load between J28-4 and J28-2
2. Enable H-Bridge 1 at 50% duty cycle with `'fb1 e=500'`
3. Read H-Bridge 1 status with `'fb1 ?'`
4. H-Bridge 1 Fault shall display "Current Limit" or "Shorted Load"
5. (optional) Power cycle to clear fault
6. Remove load from J28-4 and J28-2

H-Bridge 2:

Open Load Test:

1. Enable H-Bridge 2 at 50% duty cycle with `'fb2 e=500'`
2. Read open fault with `'fb2 ?'`
3. (optional) Power cycle to clear fault

Nominal Load Test:

4. Apply a 10Ω 150W load between J27-1 and J27-10
5. Enable H-Bridge 2 at 50% duty cycle with `'fb2 e=500'`
6. Read H-Bridge 2 current with `'fb2 ?'`
7. H-Bridge 2 current shall be 3.6A ± 0.5A
8. Disable H-Bridge 2 with `'fb2 e=0'`
9. Enable H-Bridge 2 at 50% duty cycle REVERSE with `'fb2 r=500'`
10. Read H-Bridge 2 current with `'fb2 ?'`
11. H-Bridge 2 current shall be 3.6A ± 0.5A

12. Disable H-Bridge 2 with `'fb2 r=0'`
13. Remove the 10Ω load between J27-1 and J27-10

Overcurrent Test:

1. Apply a **3Ω** 360W load between J27-1 and J27-10
2. Enable H-Bridge 2 at 50% duty cycle with `'fb2 e=500'`
3. Read H-Bridge 2 status with `'fb2 ?'`
4. Half Bridge 1 Fault shall display "Current Limit" or "Shorted Load"
5. (optional) Power cycle to clear fault
6. Remove load from J27-1 and J27-10

Low Side Drivers:

LSD 1:

Open Load Test:

1. Connect flyback path by connecting J8 to J28-27
2. Enable LSD 1 with `'lsd1 v=1800'`
3. Read open fault with `'lsd1 ?'`
4. (optional) Power cycle to clear fault

Nominal Load Test:

1. Connect flyback path by connecting J8 to J28-27
2. Apply a 10Ω 150W load between J8 and J28-26
3. Enable LSD 1 with `'lsd1 v=1800'`
4. Read LSD 1 current with `'lsd1 ?'`
5. LSD 1 current shall be 3.6A ± 0.4A
6. Disable LSD 1 with `'lsd1 v=0'`
7. Remove the 10Ω load between J8 and J28-26

Overcurrent Test:

1. Connect flyback path by connecting J8 to J28-27
2. Apply a 3Ω 360W load between J8 and J28-26
3. Enable LSD 1 with `'lsd1 v=1800'`
4. Read LSD 1 status with `'lsd1 ?'`
5. LSD 1 Fault shall display "Current Limit" or "Shorted Load"
6. (optional) Power cycle to clear fault
7. Remove load from J28-26

LSD 2:

Open Load Test:

1. Connect flyback path by connecting J8 to J27-9
2. Enable LSD 2 with `'lsd2 v=1800'`
3. Read open fault with `'lsd2 ?'`
4. (optional) Power cycle to clear fault

Nominal Load Test:

1. Connect flyback path by connecting J8 to J27-9
2. Apply a 10Ω 150W load between J8 and J27-17
3. Enable LSD 2 with `'lsd2 v=1800'`
4. Read LSD 2 current with `'lsd2 ?'`
5. LSD 2 current shall be 3.6A ± 0.4A
6. Disable LSD 2 with `'lsd2 v=0'`
7. Remove the 10Ω load between J8 and J27-17

Overcurrent Test:

1. Connect flyback path by connecting J8 to J27-9
2. Apply a 3Ω 360W load between J8 and J27-17
3. Enable LSD 2 with `'lsd2 v=1800'`
4. Read LSD 2 status with `'lsd2 ?'`
5. LSD 2 Fault shall display "Current Limit" or "Shorted Load"
6. (optional) Power cycle to clear fault
7. Remove load from J27-17

LSD 3:

Open Load Test:

1. Connect flyback path by connecting J8 to J28-10
2. Enable LSD 3 with `'lsd3 v=1800'`
3. Read open fault with `'lsd3 ?'`
4. (optional) Power cycle to clear fault

Nominal Load Test:

1. Connect flyback path by connecting J8 to J28-10
2. Apply a 10Ω 150W load between J8 and J28-1
3. Enable LSD 3 with `'lsd3 v=1800'`
4. Read LSD 3 current with `'lsd3 ?'`
5. LSD 3 current shall be 3.6A ± 0.4A

6. Disable LSD 3 with `'lsd3 v=0'`
7. Remove the 10Ω load between J8 and J28-1

Overcurrent Test:

1. Connect flyback path by connecting J8 to J28-10
2. Apply a 3Ω 360W load between J8 and J28-1
3. Enable LSD 3 with `'lsd3 v=1800'`
4. Read LSD 3 status with `'lsd3 ?'`
5. LSD 3 Fault shall display "Current Limit" or "Shorted Load"
6. (optional) Power cycle to clear fault
7. Remove load from J28-1

LSD 4:

Open Load Test:

1. Connect flyback path by connecting J8 to J28-8
2. Enable LSD 4 with `'lsd4 v=1800'`
3. Read open fault with `'lsd4 ?'`
4. (optional) Power cycle to clear fault

Nominal Load Test:

1. Connect flyback path by connecting J8 to J28-8
2. Apply a 10Ω 150W load between J8 and J28-9
3. Enable LSD 4 with `'lsd4 v=1800'`
4. Read LSD 4 current with `'lsd4 ?'`
5. LSD 4 current shall be 3.6A ± 0.4A
6. Disable LSD 4 with `'lsd4 v=0'`
7. Remove the 10Ω load between J8 and J28-9

Overcurrent Test:

1. Connect flyback path by connecting J8 to J28-8
2. Apply a 3Ω 360W load between J8 and J28-9
3. Enable LSD 4 with `'lsd4 v=1800'`
4. Read LSD 4 status with `'lsd4 ?'`
5. LSD4 Fault shall display "Current Limit" or "Shorted Load"
6. (optional) Power cycle to clear fault
7. Remove load from J28-9

LSD 5:

Open Load Test:

1. Connect flyback path by connecting J8 to J27-8
2. Enable LSD 5 with `'lsd5 v=1800'`
3. Read open fault with `'lsd5 ?'`
4. (optional) Power cycle to clear fault

Nominal Load Test:

1. Connect flyback path by connecting J8 to J27-8
2. Apply a 10Ω 150W load between J8 and J27-7
3. Enable LSD 5 with `'lsd5 v=1800'`
4. Read LSD 5 current with `'lsd5 ?'`
5. LSD 5 current shall be 3.6A ± 0.4A
6. Disable LSD 5 with `'lsd5 v=0'`
7. Remove the 10Ω load betwen J8 and J27-7

Overcurrent Test:

1. Connect flyback path by connecting J8 to J27-8
2. Apply a 3Ω 360W load between J8 and J27-7
3. Enable LSD 5 with `'lsd5 v=1800'`
4. Read LSD 5 status with `'lsd5 ?'`
5. LSD 5 Fault shall display "Current Limit" or "Shorted Load"
6. (optional) Power cycle to clear fault
7. Remove load from J27-7

LSD 6:

Open Load Test:

1. Connect flyback path by connecting J8 to J27-5
2. Enable LSD 6 with `'lsd6 v=1800'`
3. Read open fault with `'lsd6 ?'`
4. (optional) Power cycle to clear fault

Nominal Load Test:

1. Connect flyback path by connecting J8 to J27-5
2. Apply a 10Ω 150W load between J8 and J27-3
3. Enable LSD 6 with `'lsd6 v=1800'`
4. Read LSD 6 current with `'lsd6 ?'`
5. LSD 6 current shall be 3.6A ± 0.5A

6. Disable LSD 6 with ‘lsd6 v=0’
7. Remove the 10Ω load between J8 and J27-3

Overcurrent Test:

1. Connect flyback path by connecting J8 to J27-5
2. Apply a **1.5Ω** 600W load between J8 and J27-3
3. Enable LSD 6 with ‘lsd6 v=1800’
4. Read LSD 6 status with ‘lsd6 ?’
5. LSD 6 Fault shall display “Current Limit” or “Shorted Load”
6. (optional) Power cycle to clear fault
7. Remove load from J27-3

Precharge:

1. **THIS IS A 24V TEST. TURN DOWN YOUR POWER SUPPLY.**
2. Remove power from board and allow capacitance on J8 to discharge to less than <3V
3. Connect J28-17 to a **24V** 4A source with respect to COM.
4. Enable precharge with ‘precharge e=1’
5. Wait 2 seconds
6. Read bulk capacitance measurement with ‘power ?’
7. “power_BULK_Precharge_Voltage()” shall be greater than 2200
8. Measure J8 to be greater than 22V
9. Disable precharge with ‘precharge e=0’