



REV_B: Changes -

- 1) Removed I2C tie to 3p3V supply. Placed on top levels.
- 2) Switched 2 pins on Current Sense Circuit as per D3 review.
- 3) Changed 10k resistor to 4.99k resistor on Current Sense Circuit as per D3 review.
- 4) Added 1k ohm pull down resistor to Motor Control Circuit as per D3 review.
- 5) Removed the Bulk Capacitors from this design. They are added to the top level.
- 6) Changed Current limit resistor to 6.81k

D3_MOTOR_DRIVE Schematic Path = /BP_M0_2			
TENNANT			
Title Thunderbolt: D3 - COVER			
Size	Document Number	Rev	
C	<Doc>	B	
Date:	Monday, July 08, 2013	Sheet	0 of 24



REV_B: Changes -

- 1) Removed I2C tie to 3p3V supply. Placed on top levels.
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D3_MOTOR_DRIVE Schematic Path = /BP_MO_1			
TENNANT			
Title			
Thunderbolt: D3 - COVER			
Size	Document Number		Rev
C	<Doc>		B
Date:	Monday, July 08, 2013	Sheet	0 of 24

Thunderbolt Board 3-Phase Gate Drive

GAIN: (DIFF-AMP GAIN)
LOW = 10V/V
HIGH = 40V/V

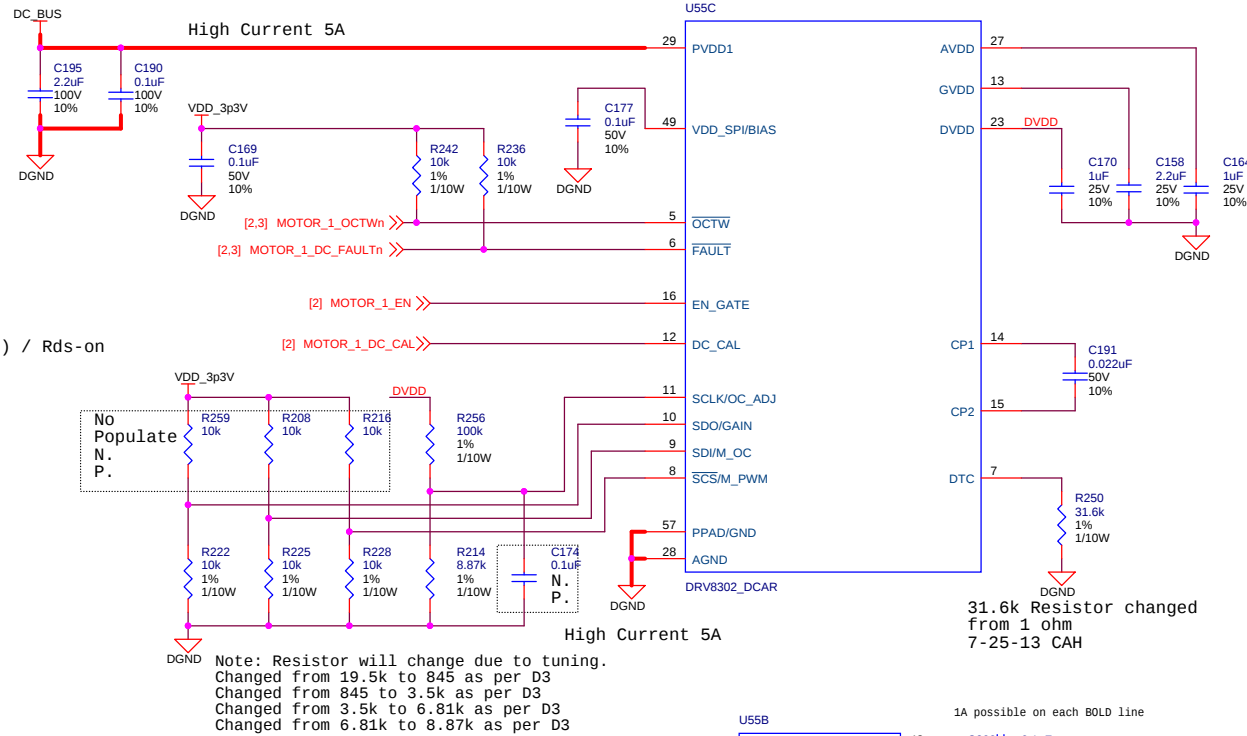
M_OC: (OVER-CURRENT PROTECTION)
LOW = CYCLE-BY-CYCLE
HIGH = LATCHED FAULT

M_PWM: (PWM MODE)
LOW = 6 - INPUT
HIGH = 3 - INPUT

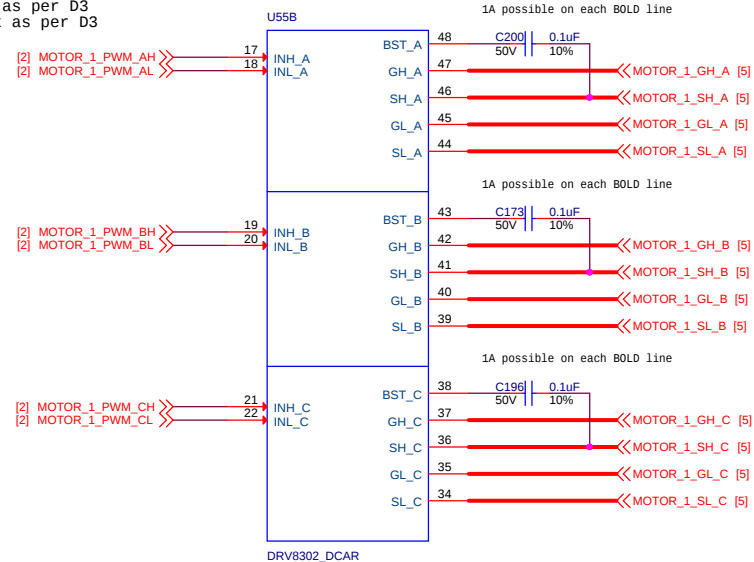
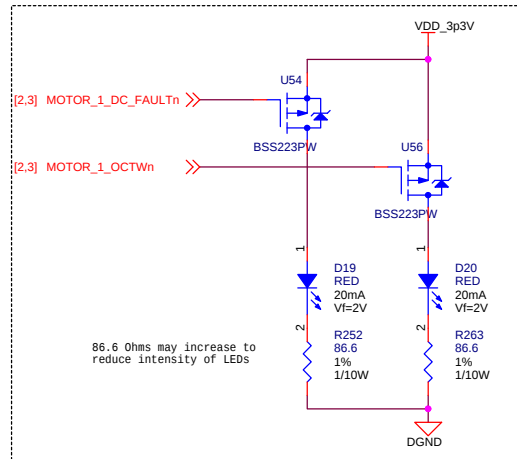
DVDD = 3.3V

M_OC = $(3.3V \cdot (19.6k / (100k + 19.6k))) / R_{ds-on}$

NOTE: GROUND RETURN PATHS ON AVDD, GVDD, DVDD
ARE VERY IMPORTANT. SEE TI APP NOTE: SLVA552



OPTIONAL FAULT INDICATION LEDS

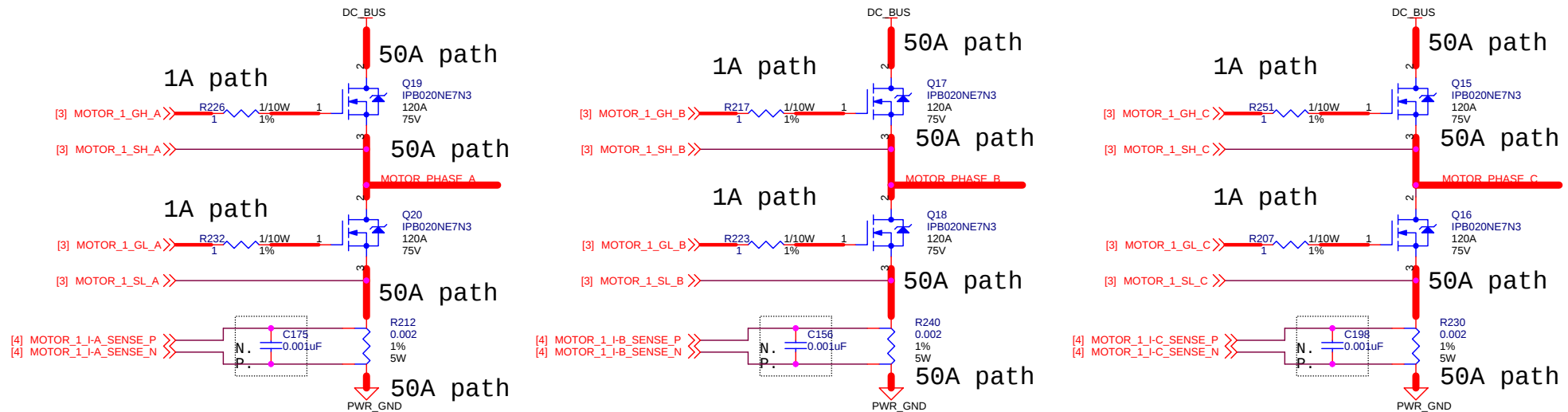


D3_MOTOR_DRIVE Schematic Path = /3P_MD_2

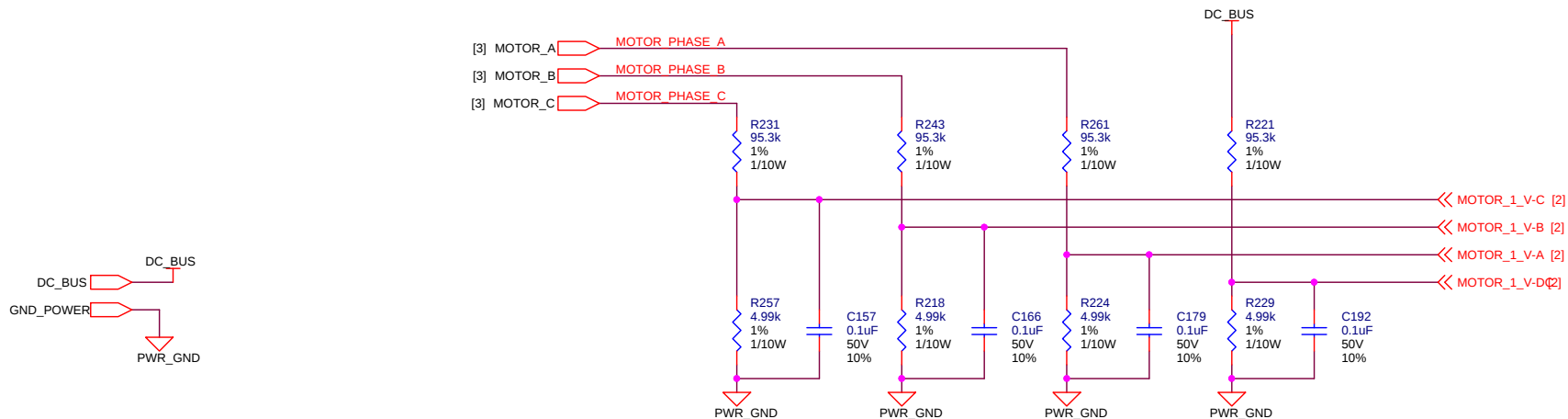
TENNANT		
Title		
Thunderbolt: D3 - GATE DRIVE		
Size	Document Number	Rev
Custom-Doc		B
Date:	Wednesday, September 25, 2013	Sheet 0 of 24

Thunderbolt Board

3-Phase Motor H-Bridge



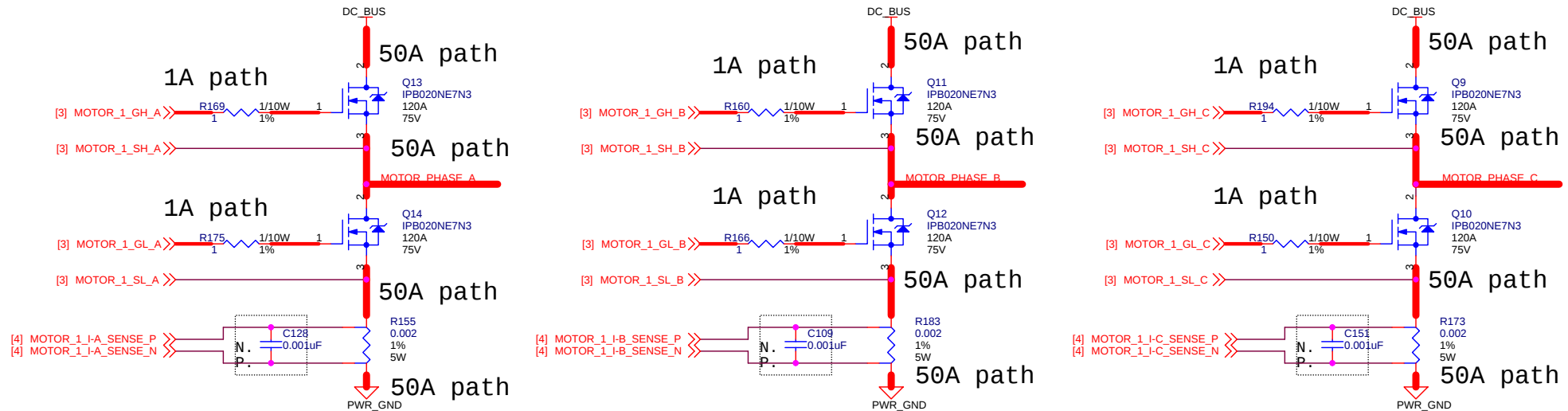
NOTE: KELVIN CONNECTIONS REQUIRED ON SENSE RESISTOR (3) PLCS



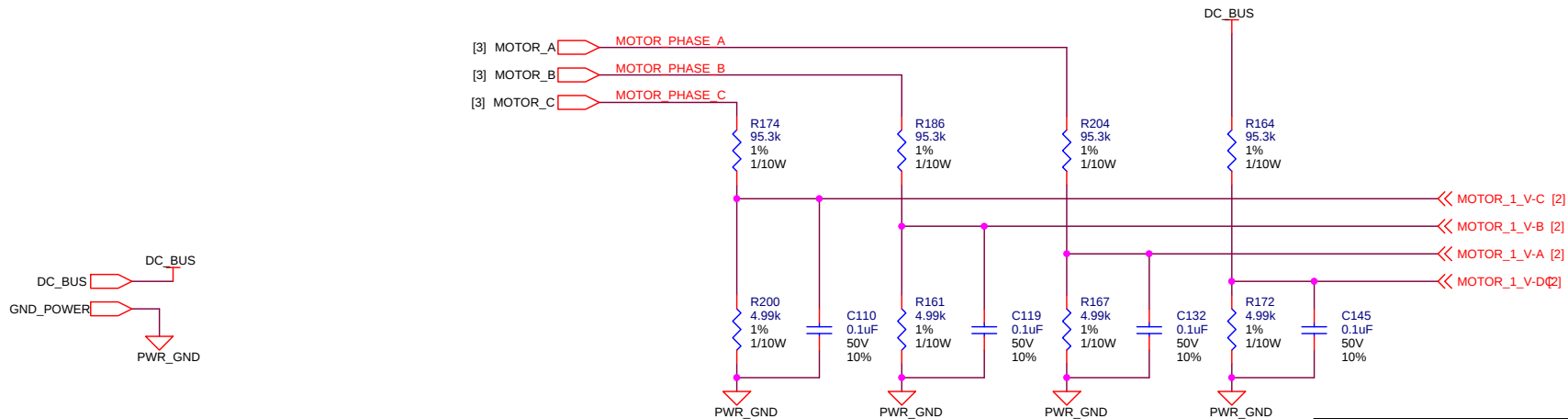
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Title Thunderbolt: D3 - MOTOR H-BRIDGE		
Size Custom	Document Number	Rev B
Date: Friday, September 20, 2013	Sheet 0 of 24	

Thunderbolt Board

3-Phase Motor H-Bridge



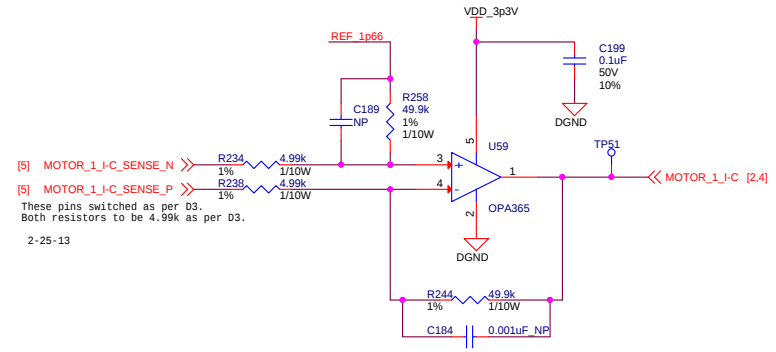
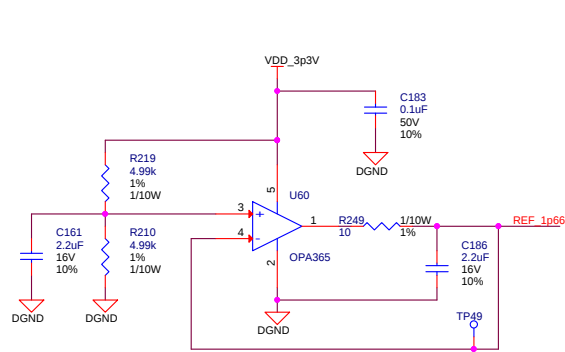
NOTE: KELVIN CONNECTIONS REQUIRED ON SENSE RESISTOR (3) PLCS



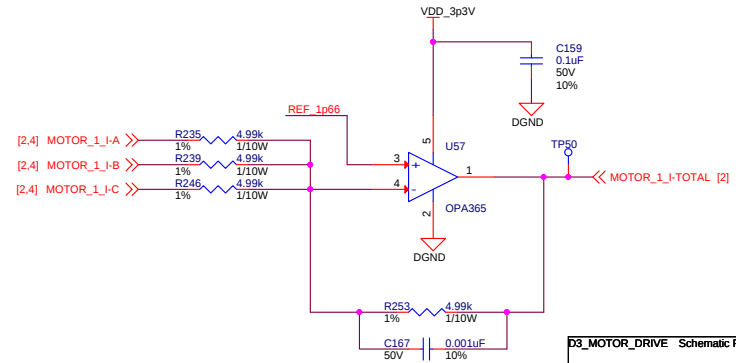
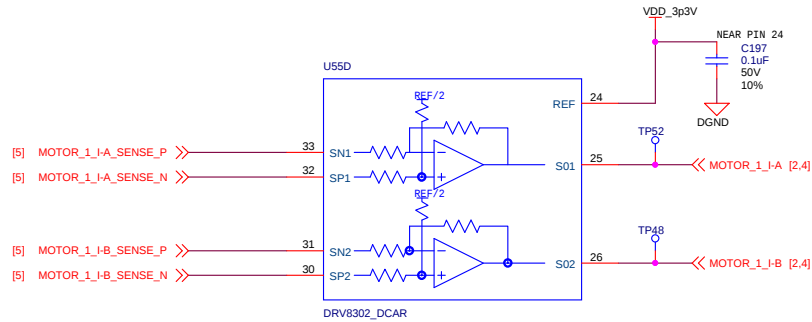
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Thunderbolt: D3 - MOTOR H-BRIDGE		
Size	Document Number	Rev
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Date:	Friday, September 20, 2013	Sheet 0 of 24

Thunderbolt Board

3-Phase Current Sense



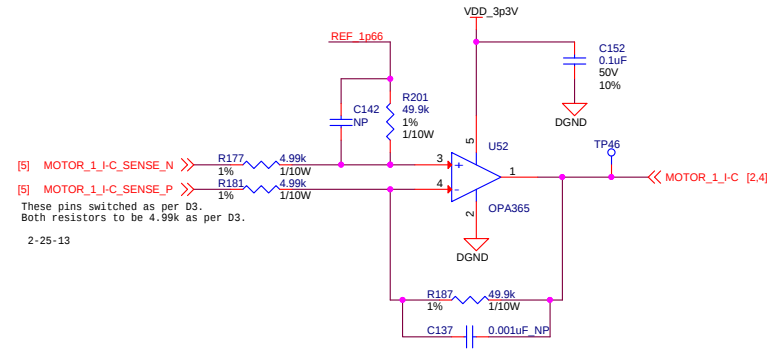
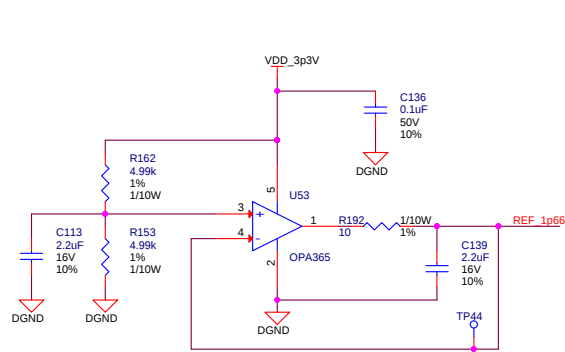
GAIN = 10 V/V



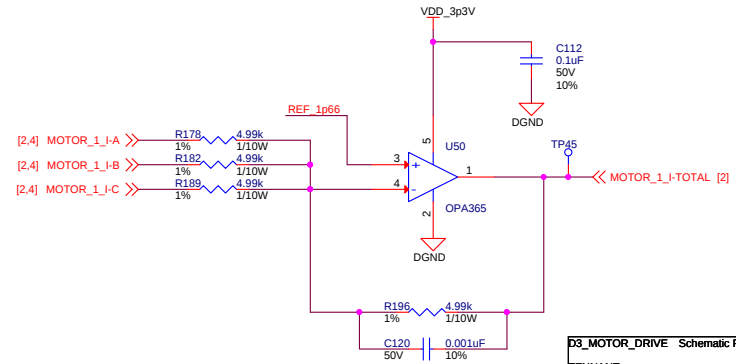
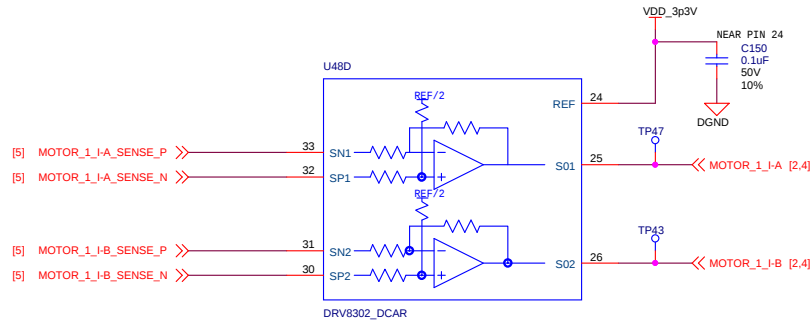
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Size	Document Number	Rev	
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Date:	Friday, September 20, 2013	Sheet	0 of 24

Thunderbolt Board

3-Phase Current Sense



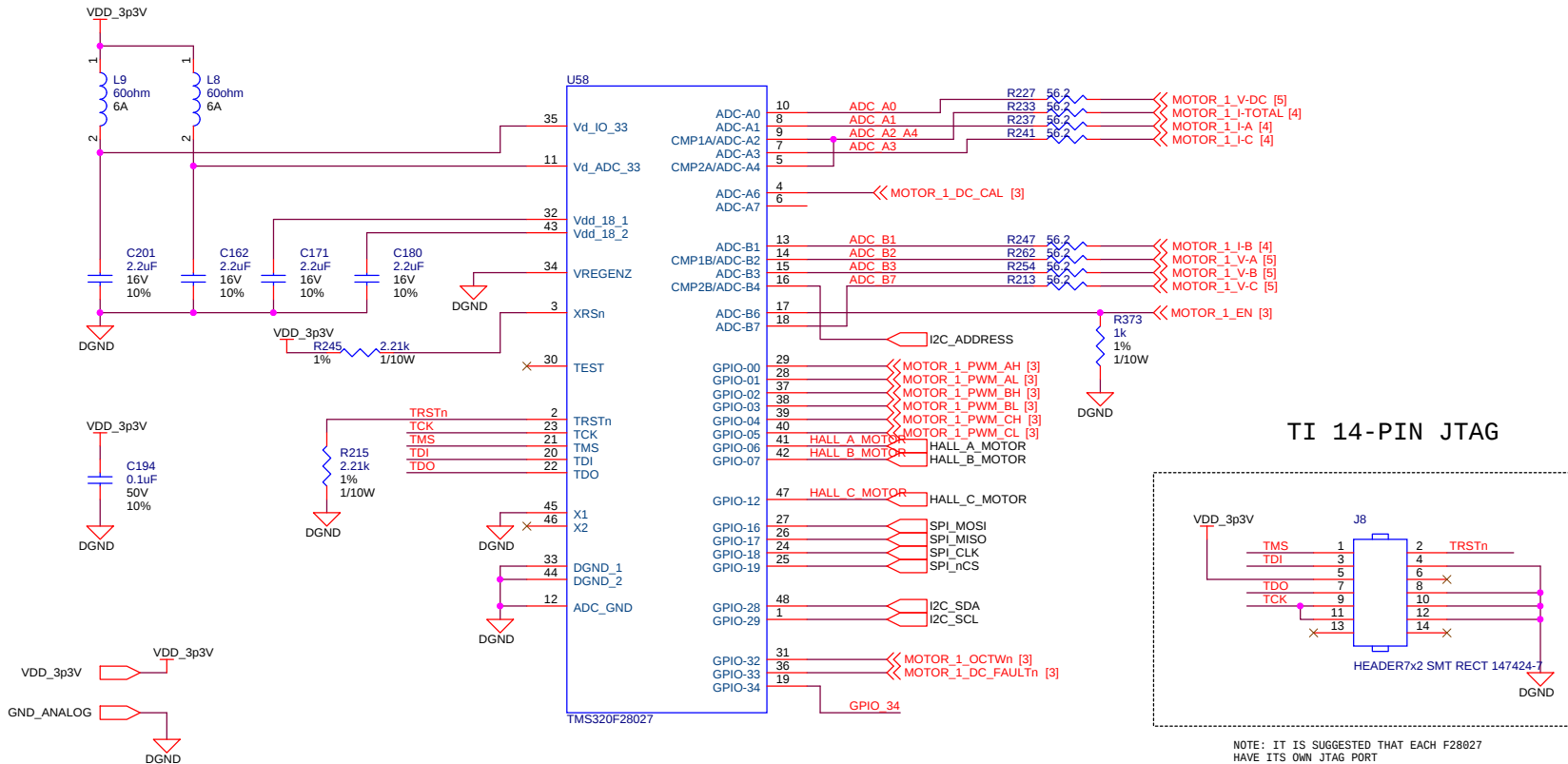
GAIN = 10 V/V



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Thunderbolt: D3 - CURRENT SENSE			
Size	Document Number	Rev	
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Date:	Friday, September 20, 2013	Sheet	0 of 24

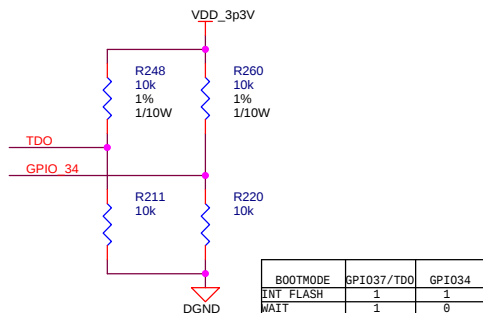
Thunderbolt Board

3-Phase Motor Control



NOTE: IT IS SUGGESTED THAT EACH F28027 HAVE ITS OWN JTAG PORT

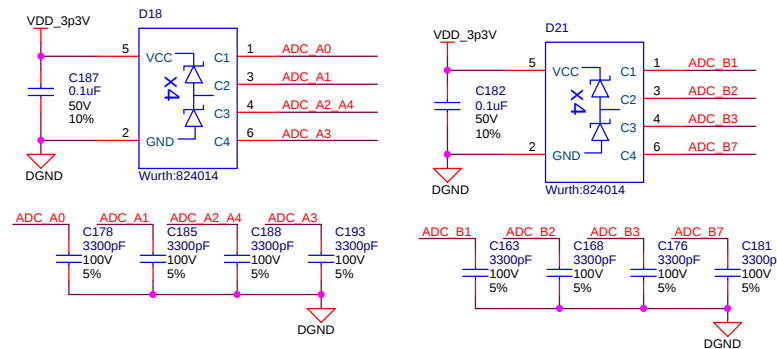
Boot-mode Selection



BOOTMODE	GPIO37/TDO	GPIO34
INT_FLASH	1	1
WAIT	1	0
SCI-A	0	1
PARALLEL IO	0	0

NOTE: WAIT STATE IS USED IF DEBUGGING WITH CODE SECURITY TURNED ON IS NEEDED

NOTE: JTAG WILL ASSERT TRSTn PIN TO ENTER EMU BOOT MODE (SEE PAGE 24 OF 28027 DATASHEET)



D3_MOTOR_DRIVE Schematic Path = /3P_MD_2

TENNANT

Title
Thunderbolt: D3 - MOTOR CONTROL DSP

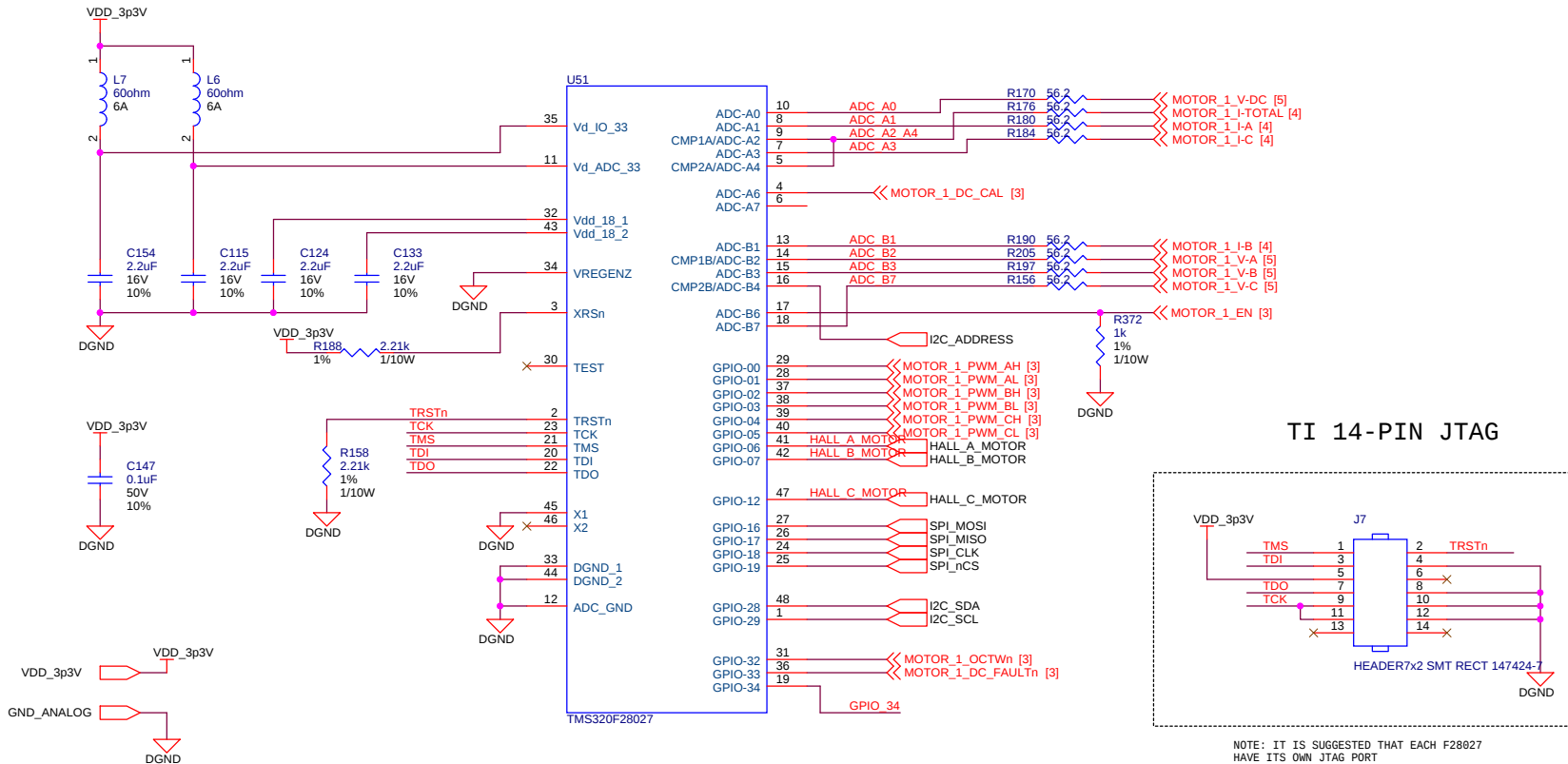
Size Document Number
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Rev
B

Date: Wednesday, September 25, 2013 Sheet 0 of 24

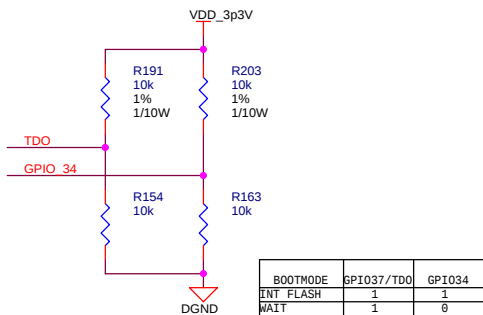
Thunderbolt Board

3-Phase Motor Control



NOTE: IT IS SUGGESTED THAT EACH F28027 HAVE ITS OWN JTAG PORT

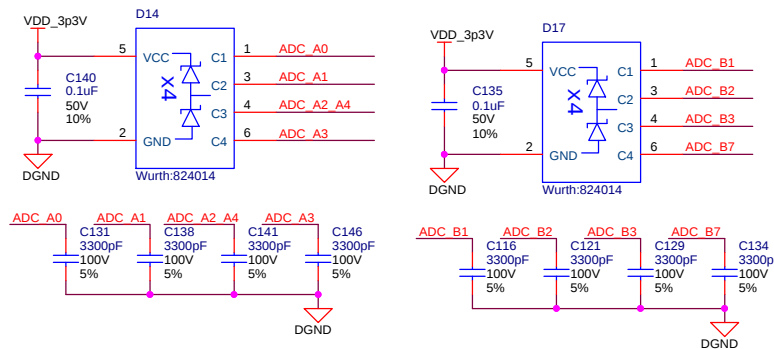
Boot-mode Selection



BOOTMODE	GPIO37/TDO	GPIO34
INT_FLASH	1	1
WAIT	1	0
SCI-A	0	1
PARALLEL IO	0	0

NOTE: WAIT STATE IS USED IF DEBUGGING WITH CODE SECURITY TURNED ON IS NEEDED

NOTE: JTAG WILL ASSERT TRSTn PIN TO ENTER EMU BOOT MODE (SEE PAGE 24 OF 28027 DATASHEET)



D3_MOTOR_DRIVE Schematic Path = /3P_MD_1

TENNANT

Title
Thunderbolt: D3 - MOTOR CONTROL DSP

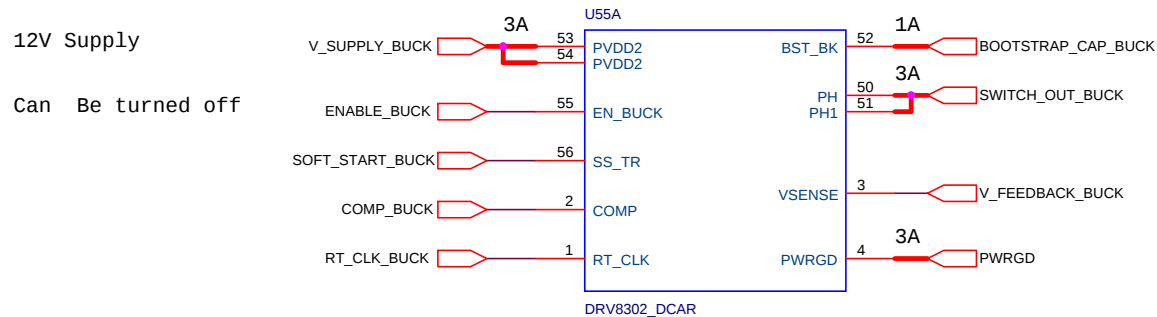
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Rev
B

Date: Wednesday, September 25, 2013 Sheet 0 of 24

Thunderbolt Board

3-Phase Motor OPTIONAL BUCK



NOTE: DRV8302 HAS THE SAME BUCK
CONVERTER AS THE TPS54160

INFO TAKEN FROM DATA SHEET

RT_CLK 1 I Resistor timing and external clock for buck regulator. Resistor should connect to GND (power pad) with very short trace to reduce the potential clock jitter due to noise.

COMP 2 0 Buck error amplifier output and input to the output switch current comparator.

VSENSE 3 I Buck output voltage sense pin. Inverting node of error amplifier.

PWRGD 4 I An open drain output with external pull-up resistor required. Asserts low if buck output voltage is low due to thermal shutdown, dropout, over-voltage, or EN_BUCK shut down

BST_BK 52 P Bootstrap cap pin for buck converter

PVDD2 53,54 P Power supply pin for buck converter, PVDD2 cap should connect to GND.

EN_BUCK 55 I Enable buck converter. Internal pull-up current source. Pull below 1.2V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors

SS_TR 56 I Buck soft-start and tracking. An external capacitor connected to this pin sets the output rise time. Since the voltage on this pin overrides the internal reference, it can be used for tracking and sequencing. Cap should connect to GND

GND 57 P GND pin. The exposed power pad must be electrically connected to ground plane through soldering to (POWER PCB for proper operation and connected to bottom side of PCB through vias for better thermal PAD) spreading.

D3_MOTOR_DRIVE Schematic Path = /3P_MD_2

TENNANT

Title

Thunderbolt: D3 - POWER BUCK - OPTIONAL

Size

Document Number

Rev

Custom<Doc>

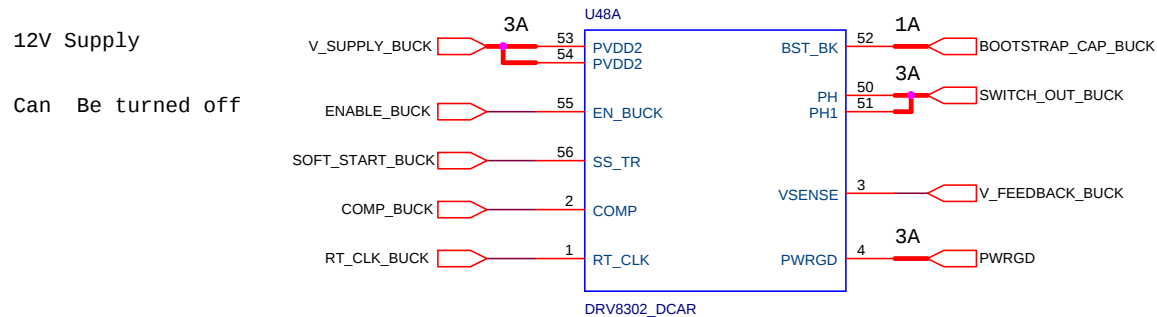
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Date: Monday, July 22, 2013

Sheet 0 of 24

Thunderbolt Board

3-Phase Motor OPTIONAL BUCK



NOTE: DRV8302 HAS THE SAME BUCK
CONVERTER AS THE TPS54160

INFO TAKEN FROM DATA SHEET

RT_CLK 1 I Resistor timing and external clock for buck regulator. Resistor should connect to GND (power pad) with very short trace to reduce the potential clock jitter due to noise.

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VSENSE 3 I Buck output voltage sense pin. Inverting node of error amplifier.

PWRGD 4 I An open drain output with external pull-up resistor required. Asserts low if buck output voltage is low due to thermal shutdown, dropout, over-voltage, or EN_BUCK shut down

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GND 57 P GND pin. The exposed power pad must be electrically connected to ground plane through soldering to (POWER PCB for proper operation and connected to bottom side of PCB through vias for better thermal PAD) spreading.

D3_MOTOR_DRIVE Schematic Path = /3P_MD_1

TENNANT

Title

Thunderbolt: D3 - POWER BUCK - OPTIONAL

Size

Document Number

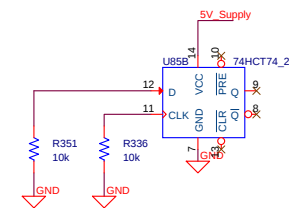
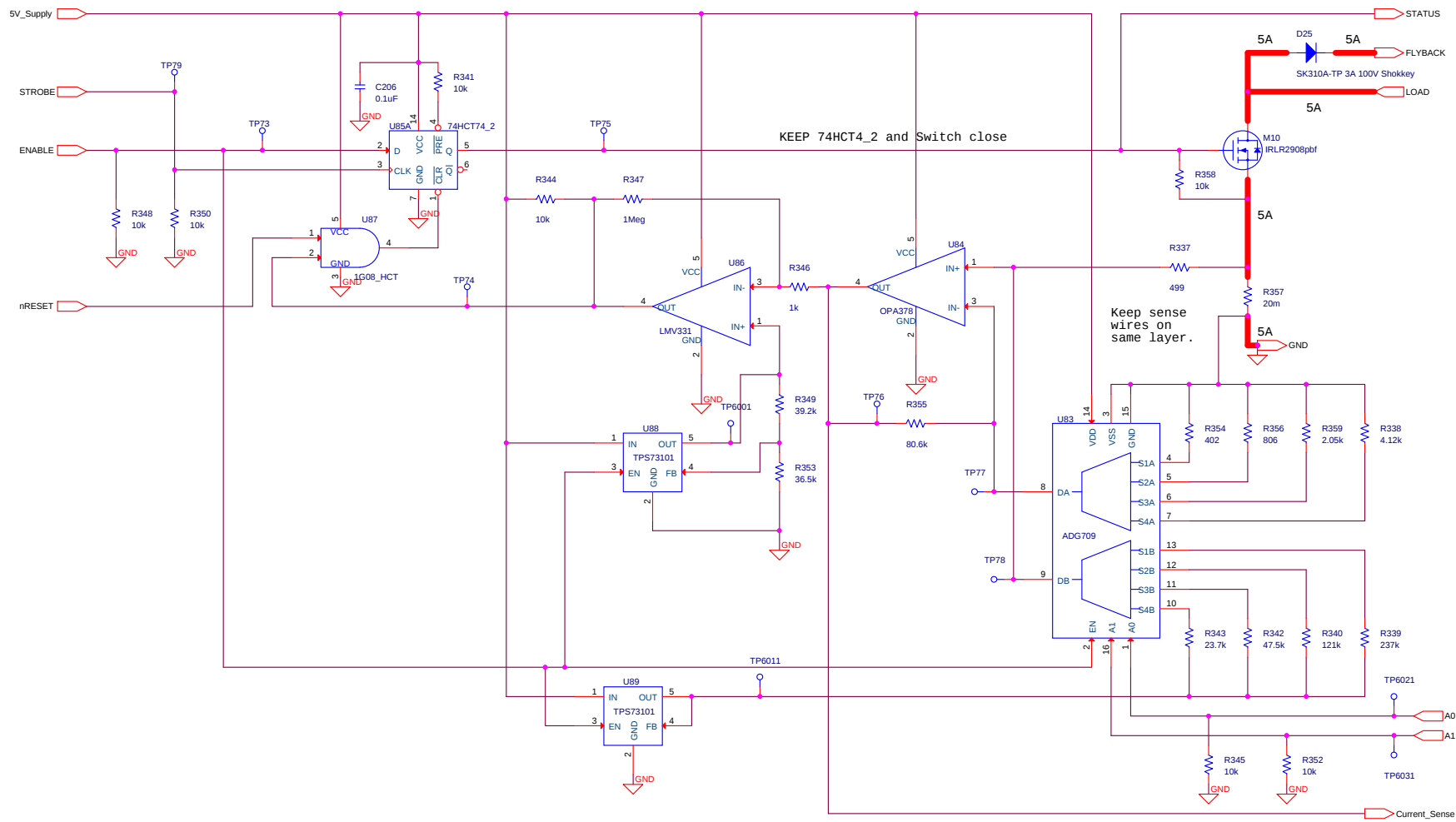
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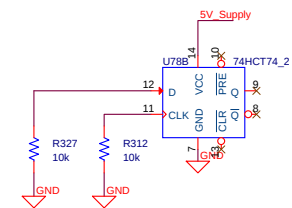
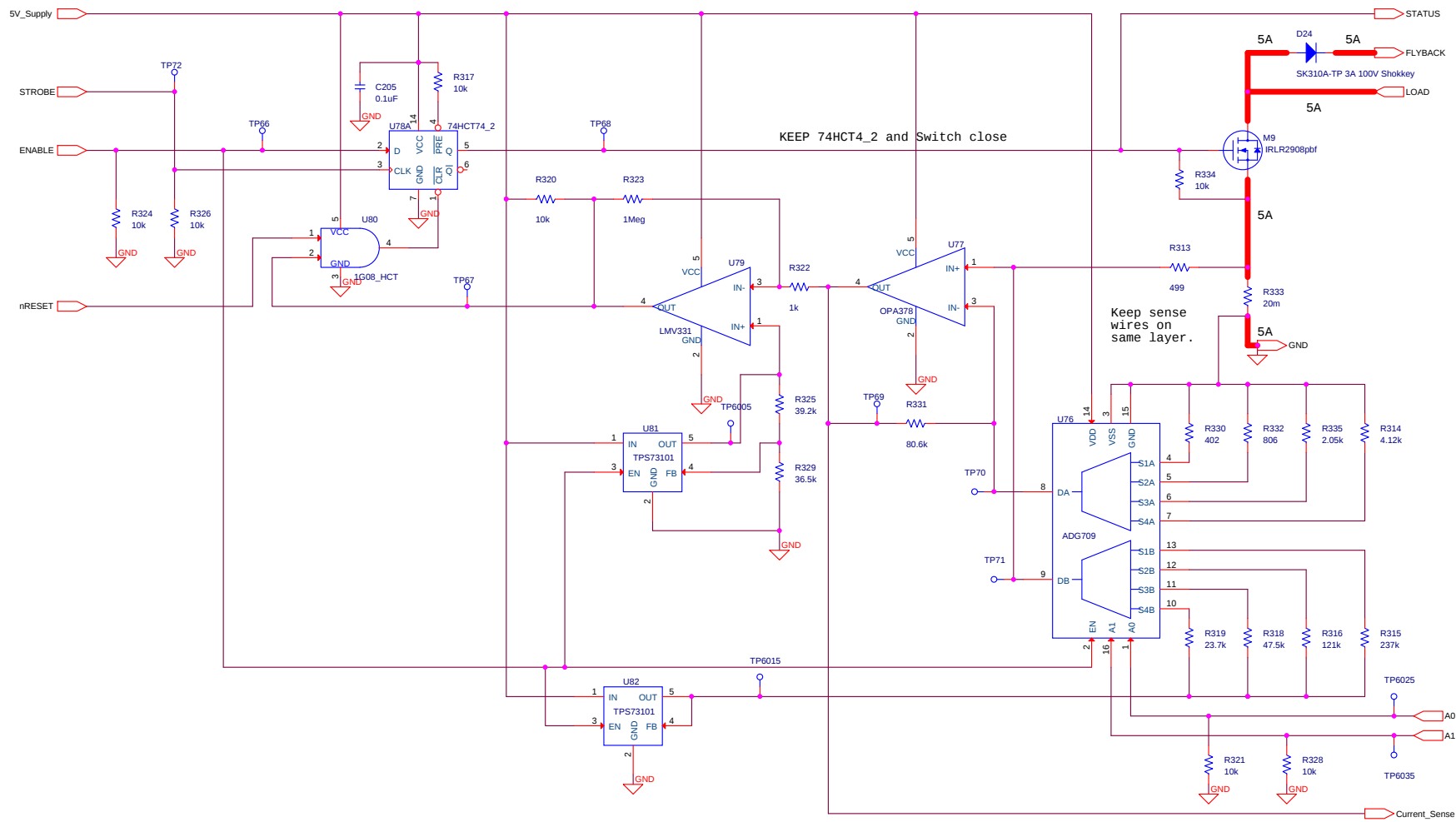
Date: Monday, July 22, 2013

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REV_B: Changes -
1) Changed Schottkey to 3A (80A non-repetitive peak) Diode

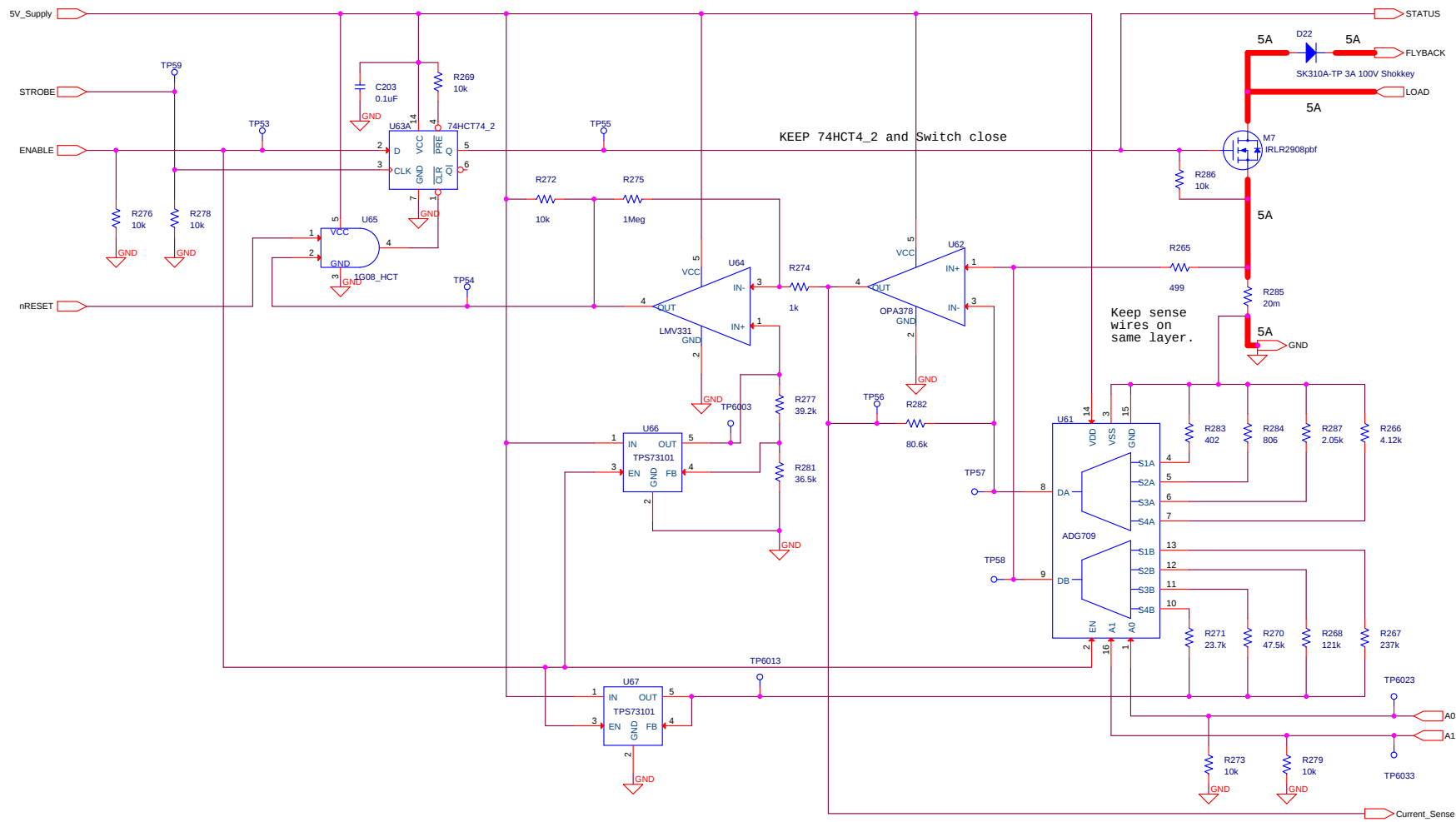
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Low Side Driver Circuit		
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Size	Document Number	Rev
CustomerDoc =		B
Date:	Monday, September 23, 2013	Sheet 0 of 24



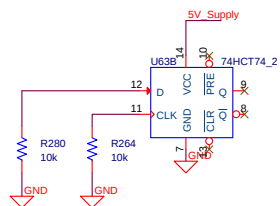
REV_B: Changes -
1) Changed Schottkey to 3A (80A non-repetitive peak) Diode

LS2 Schematic Path = /LS2
Low Side Driver Circuit
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Size	Document Number	Rev
CustomerDoc =		B
Date:	Monday, September 23, 2013	Sheet 0 of 24



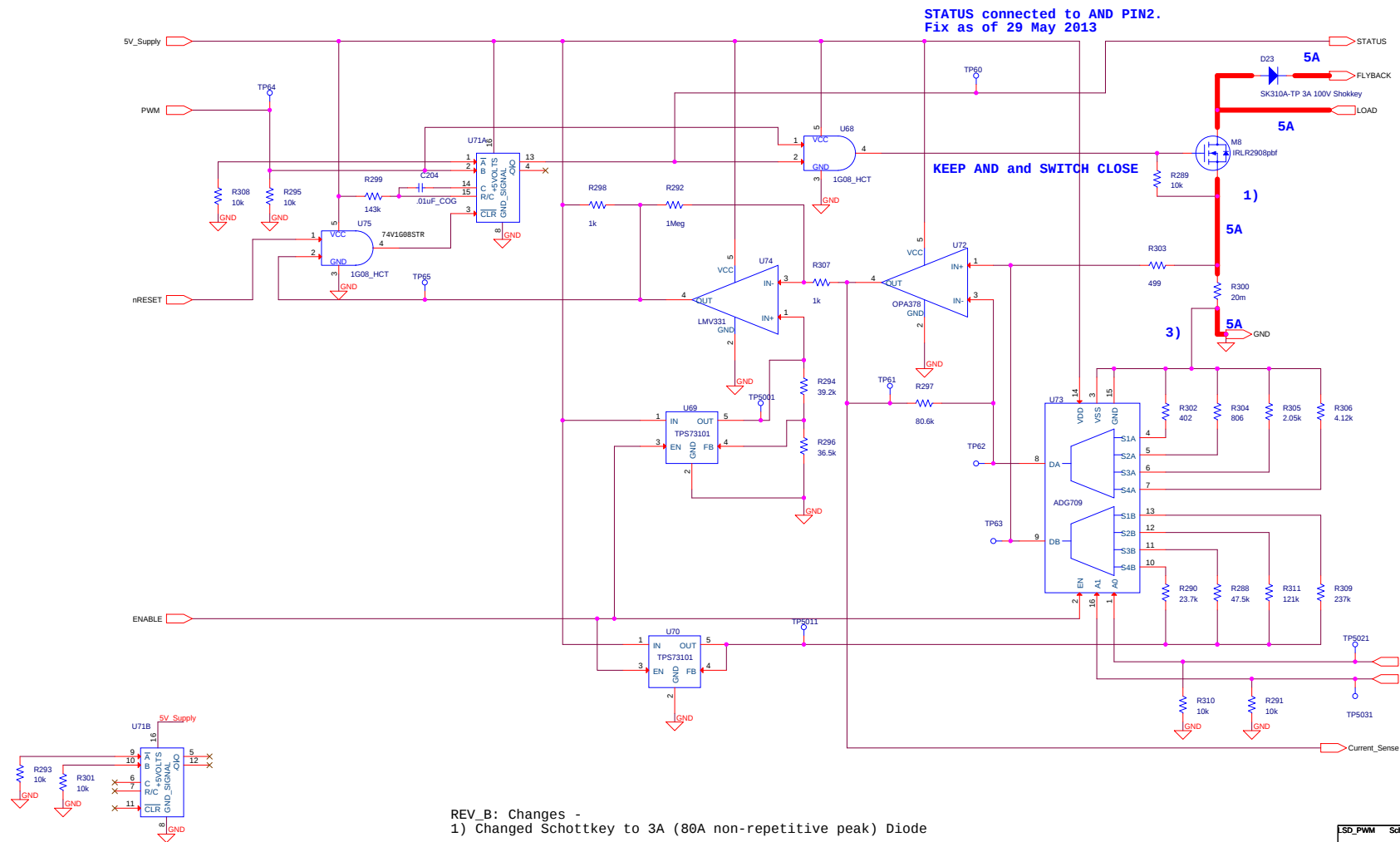
REV_B: Changes -
 1) Changed Schottkey to 3A (80A non-repetitive peak) Diode



LSD Schematic Path = /LSD1			
Low Side Driver Circuit			
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Size	Document Number		
CustomerDoc =			
Date:	Monday, September 23, 2013	Sheet	0 of 24
			Rev B

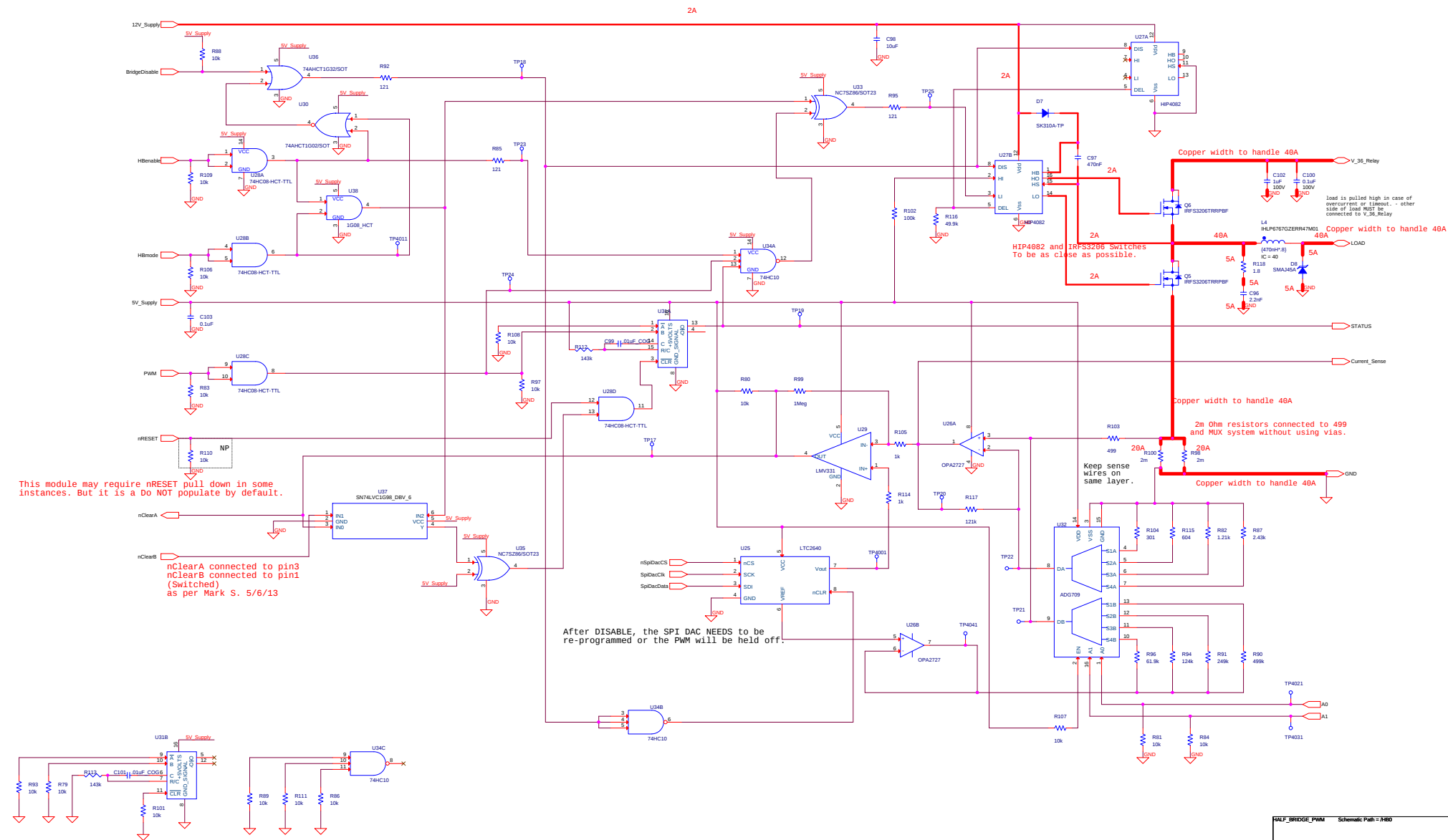
LAYOUT NOTES

- 1) Cu 250mils wide. ~ 10A capability
- 2) All Resistors at 1% Except 1Meg and 10k ohm Resistors can be 5%
- 3) R5-R8 tied directly to R3 on TOP LEVEL before via to ground. USE MANY VIAS to ground out this node.



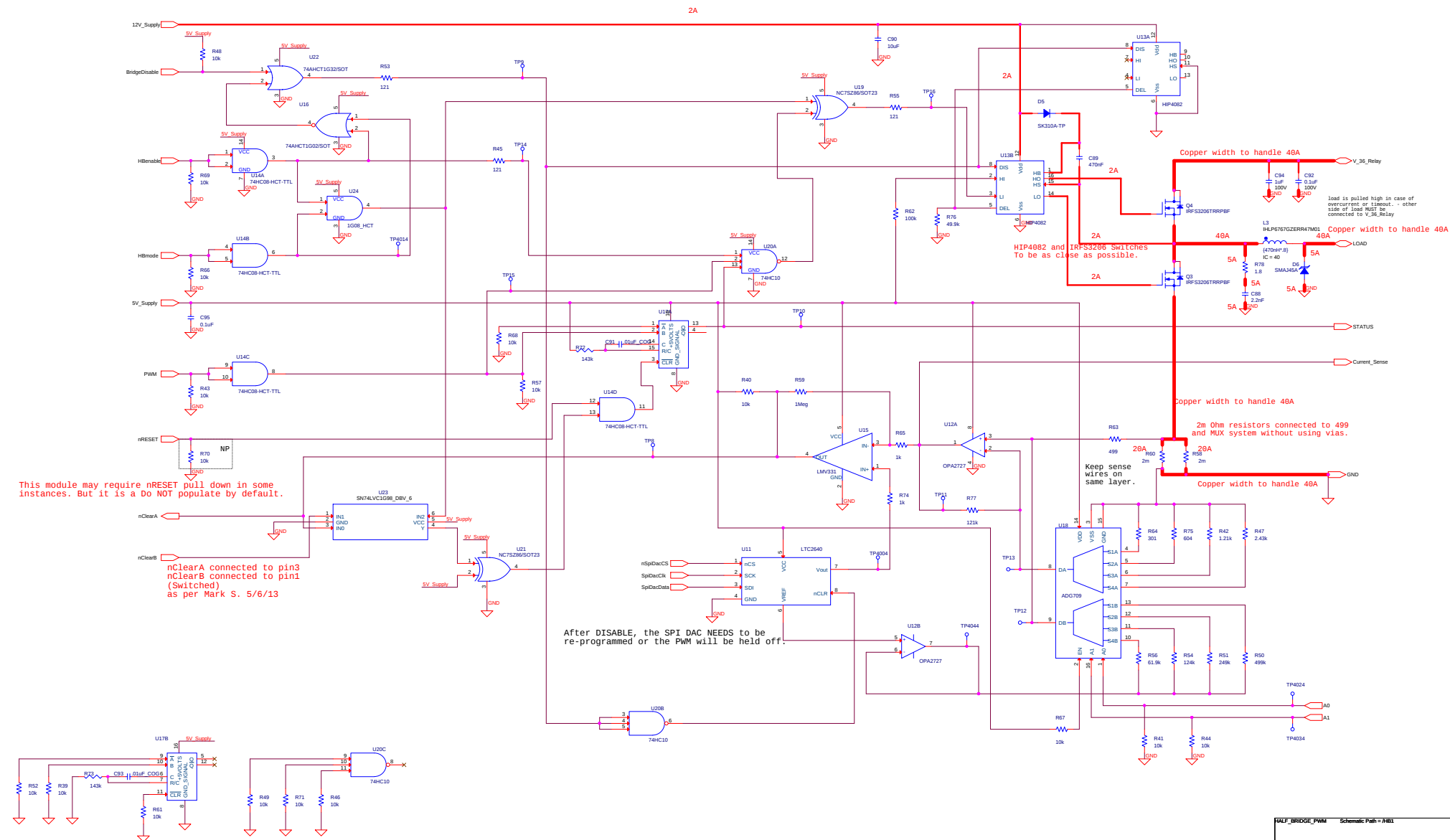
LAYOUT NOTES

- 1) Cu 250mils wide. ~ 10A capability. Need ~40A capability @ 1 oz Cu. May change for 2 oz Cu.
- 2) All Resistors at 1% Except 1Meg ohm Resistors can be 5% if no 1% available.
- 3) 2m Ohm resistors tied directly to 499 ohms on TOP LEVEL before via to ground. USE MANY VIAS to ground out this node.
- 4) To minimize ringing in the bootstrap circuit, keep the PCB traces from the HIP4082 to the external bootstrap capacitor and MOSFETs as short as possible. The bypass capacitor should be located as close as possible to the IC. Ceramic dielectric is the best choice for bypass and bootstrap capacitors.

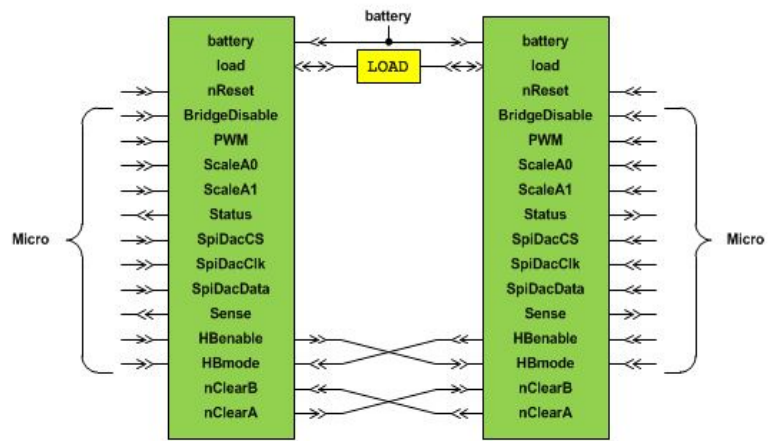


LAYOUT NOTES

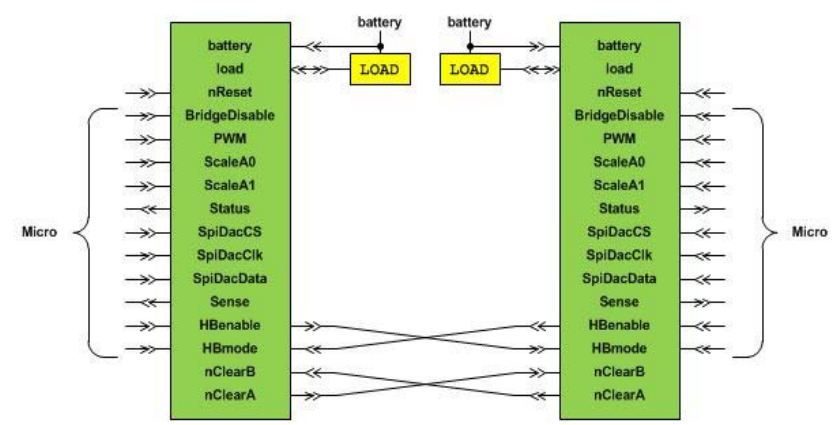
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- 2) All Resistors at 1% Except 1Meg ohm Resistors can be 5% if no 1% available.
- 3) 2m Ohm resistors tied directly to 499 ohms on TOP LEVEL before via to ground. USE MANY VIAS to ground out this node.
- 4) To minimize ringing in the bootstrap circuit, keep the PCB traces from the HIP4082 to the external bootstrap capacitor and MOSFETs as short as possible. The bypass capacitor should be located as close as possible to the IC. Ceramic dielectric is the best choice for bypass and bootstrap capacitors.



APP NOTES

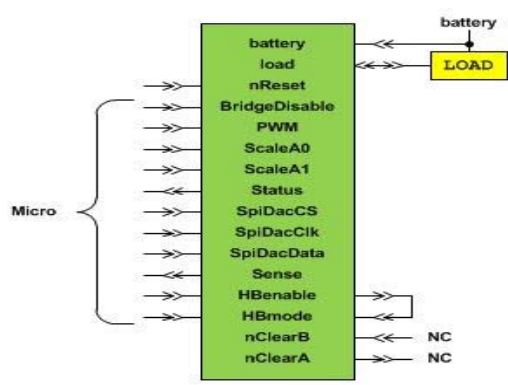


H-Bridge Application



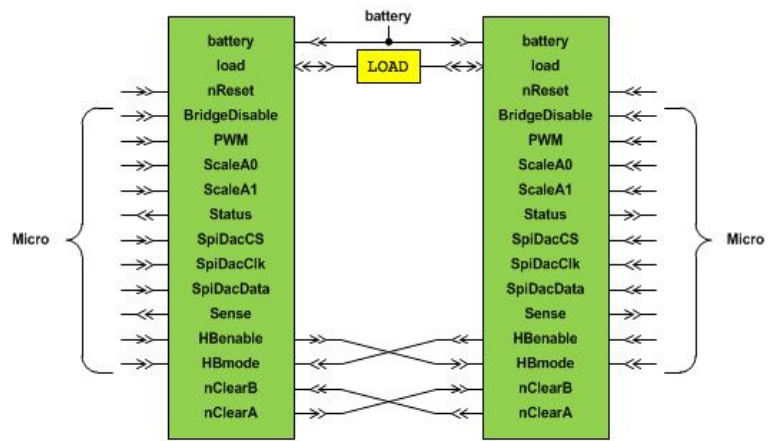
2 Half Bridge Application

Update: BridgeDisable Pull up to 5V to solve Startup issues. 9-19-13

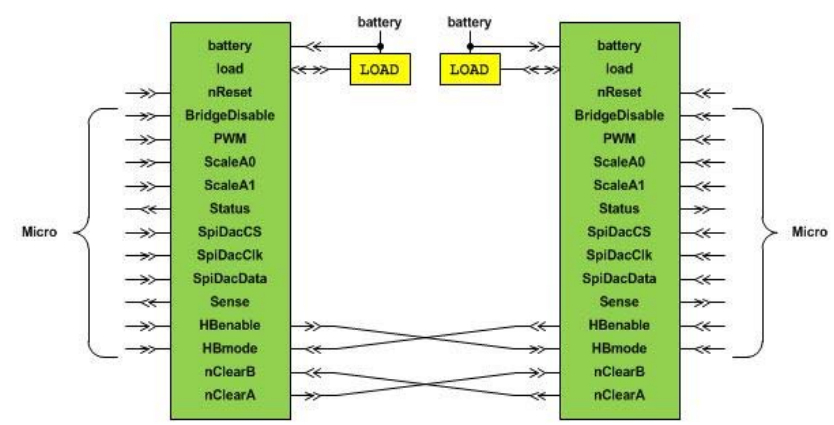


Half-Bridge Application

APP NOTES

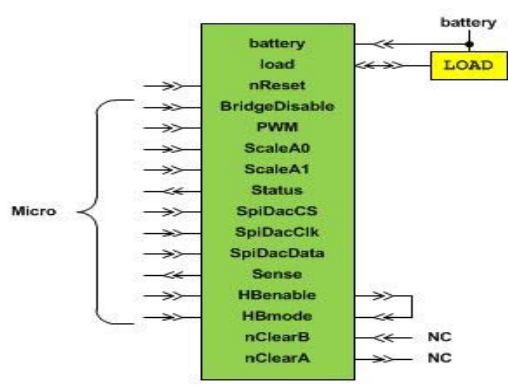


H-Bridge Application



2 Half Bridge Application

Update: BridgeDisable Pull up to 5V to solve Startup issues. 9-19-13



Half-Bridge Application



Rev B - Changes :

- 1) added 2 OR chips and 1 NOR chip for SPI chip select of the D3 Motor Drivers, added on the 2 - TOP LEVEL MAIN SCRUB SCHEMATIC
- 2) added Footprint for J9
- 3) changed 80A Reference to 100A Reference to 4 - POWER SUPPLIES SCHEMATIC

Rev C - Changes :

- 1) An issue was found with the off page reference connectors. They were all adjusted to fix this issue
- 2) Half Bridge Resistor and Capacitor changed for better thermal stability.
- 3) COIL GND PIN REMOVED.

Rev D - Changes :

- 1) Changed Diodes in Low Side Driver (LSD) circuits to make for better room and routing in layout.
- 2) Switched A and C on Motor 2 for 3 phase to help with Layout Placement.

Rev E - Changes :

- 1) Changed U90 Top level to U93 due to duplicate part number.
- 2) Corrected Footprints on J1, J4, U9, (U69/U70 from LSDP0)

Rev F - Changes :

- 1) JTAG for the 3 Phase Motor Circuit Female PCB connector is compatible with our current tools.

Rev G - Changes :

- 1) SPI pull up resistors changed from 10k to 1k. SPI connections on 3-Phase TX/RX switched.
Changed Capacitors for BUS to 820uF through hole parts.
- 2) Added 4th pin for N-Channel devices for layout help in HB.

Rev H - Changes to facilitate layout.

- 1) Buck circuit components switched on 3- Drivers D3 and Tennant. This will help with where components are placed.

Rev J - Changes :

- 1) Changed a few of Micro pins.
- 2) Added I2C and pull up resistors to Micro and D3 Motors

Rev K - Changes :

- 1) A few of the QPLnumbers/footprints were wrong. Fixed.
- 2) 2 pins switched on micro.
- 3) Precharge has been modified to allow Curtis to control the Relay.

Rev L - Changes :

- 1) Fixed a mis-wired circuit in precharge.

Rev M - Changes :

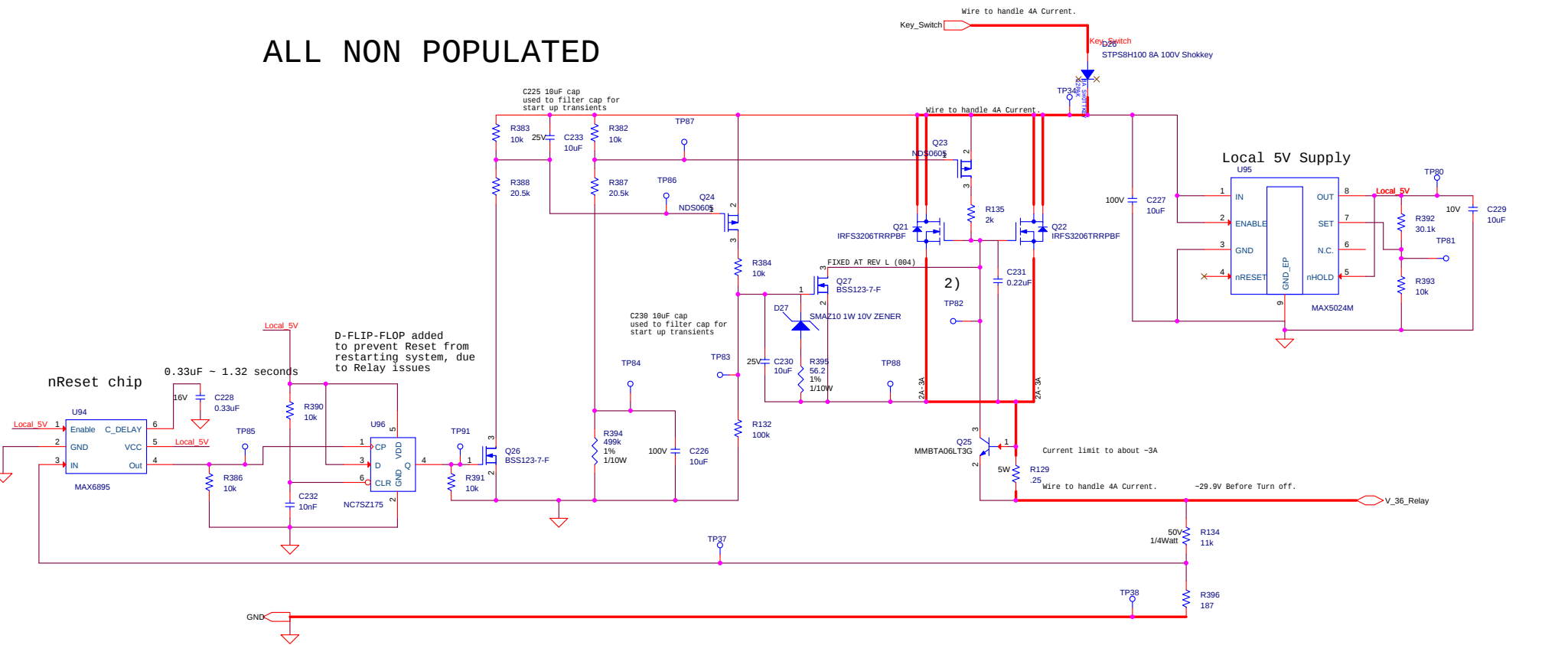
- 1) De-pop'd pre-charge

Rev N - Changes :

- 1) Fixed power supply diode, D3, sheet 3

TENNANT			
Title			
Thunderbolt: Main Scrub Board			
Size	Document Number	Rev	
Customer	Doc#	N	
Date:	Tuesday, April 01, 2014	Sheet	1 of 16

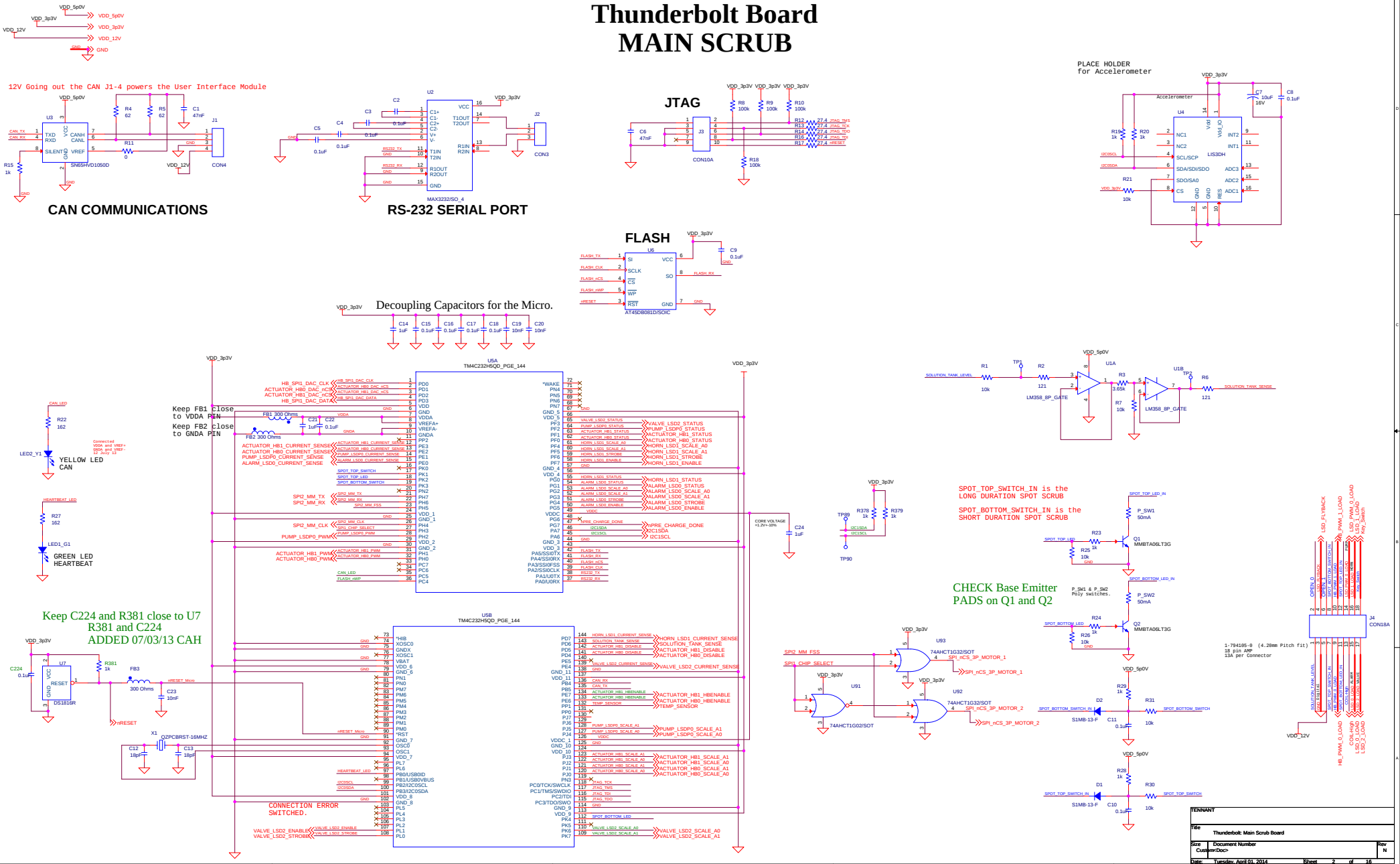
ALL NON POPULATED



PRECHARGE		
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Size	Document Number	Rev
Custom	Doc	?
Date	Monday, March 10, 2014	Sheet 1 of 24

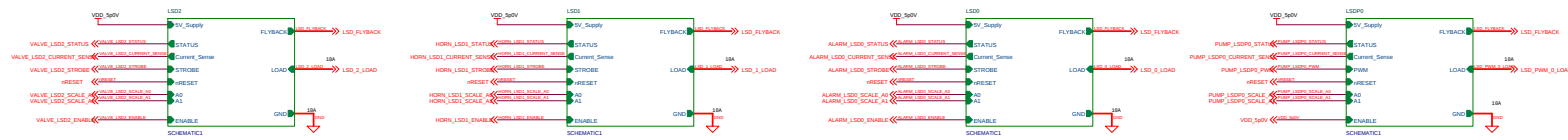
Thunderbolt Board

MAIN SCRUB

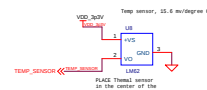


MAIN SCRUB: DRIVERS AND SWITCHES

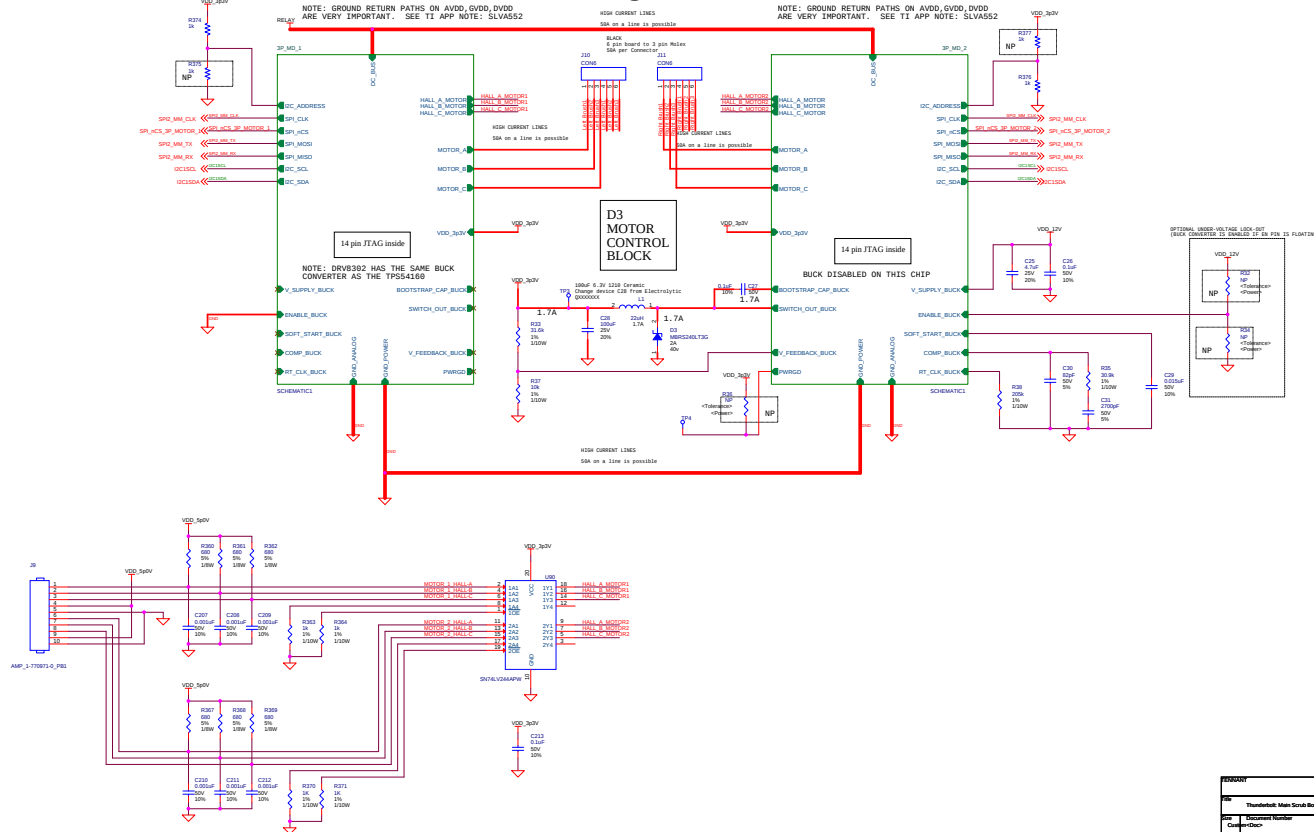
Low Side Drivers



H-Bridge Drivers

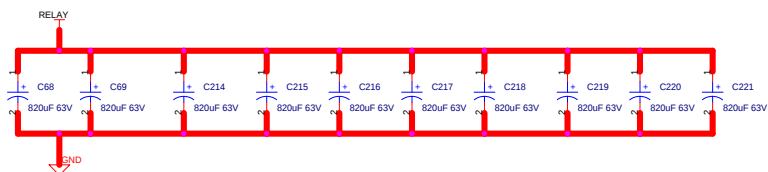


3Phase H-Bridge Drivers

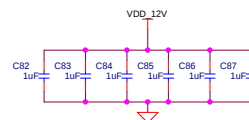
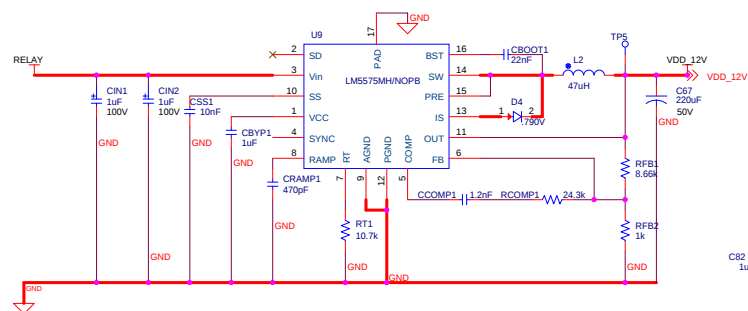
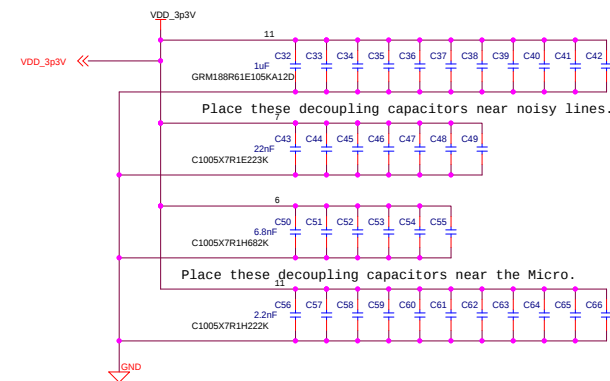


3.3V

12V



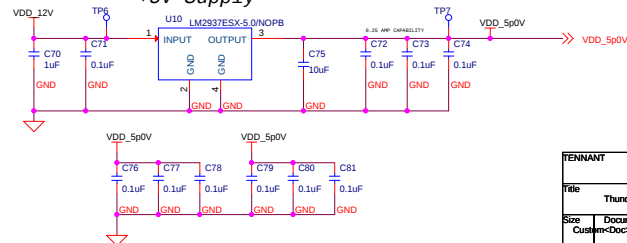
~100 AMPS



5V

NOTE: 5V RAIL NOT NEEDED BY MOTOR CONTROLLER

+5V Supply



TENNANT			
Title Thunderbolt: Main Scrub Board - Drivers			
Size Custom<Doc>	Document Number		Rev N
Date:	Tuesday, April 01, 2014	Sheet	4 of 16

Hall Sensors Removed and placed on the Top Level
Schematic due to the fact that we have part of the
design needing 2 and part needing 1.

D3_MOTOR_DRIVE Schematic Path = /BP_M0_2	
TENNIANT	
Title	
Thunderbolt: D3 - Hall Sensors	
Size	Document Number
C	<Doc>
Date:	Monday, March 25, 2013
Sheet	6 of 7
1	

Hall Sensors Removed and placed on the Top Level
Schematic due to the fact that we have part of the
design needing 2 and part needing 1.

D3_MOTOR_DRIVE Schematic Path = /BP_MD_1	
TENNANT	
Title	
Thunderbolt: D3 - Hall Sensors	
Size	Document Number
C	<Doc>
Date:	Monday, March 25, 2013
Sheet	6 of 7
1	