

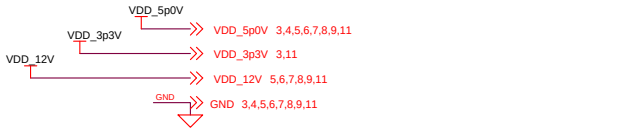


Q26015-005
MAIN SWEEP

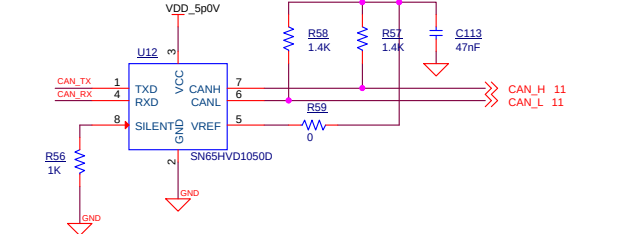
- REV- - INITIAL RELEASE
- 001 - Inital Release
 - 002 - Added filtering for A/D and for Slew rate for hot temps.
Changed 5A actuator FETs to smaller FET types.
Multiple changes in references to help Layout (A-G)
 - 003 - Added 2 NON-POP DISCHARGE RESISTORS TO DECREASE DISCHARGE TIME.
Changed JTAG CLOCK RESISTOR TO PULL DOWN. (H)
 - 004 - Changed Roll Actuator to be 6.93A Limit (J)
 - 005 - Changed Roll Actuator to be 9.91A Limit (K)
 - 006 - Changed Shaker to be 10.05A limit (L)
 - 007 - Updated rev bits to "1". (M)

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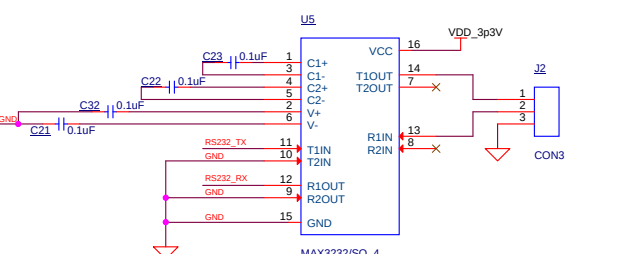
MAIN SWEEP BOARD MICRO AND COMMUNICATIONS



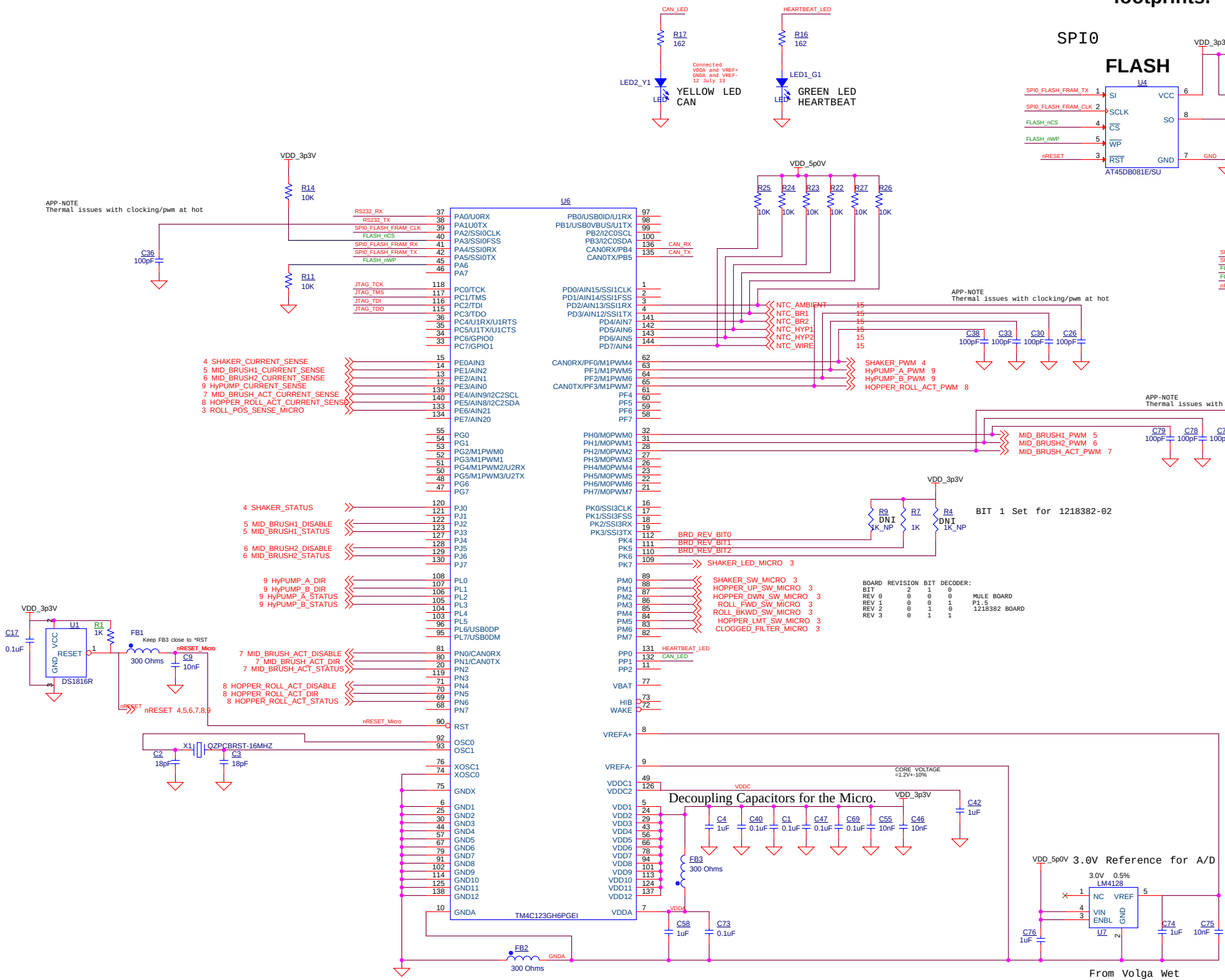
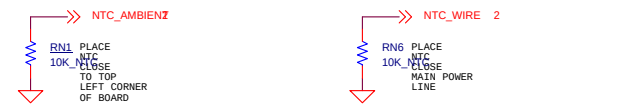
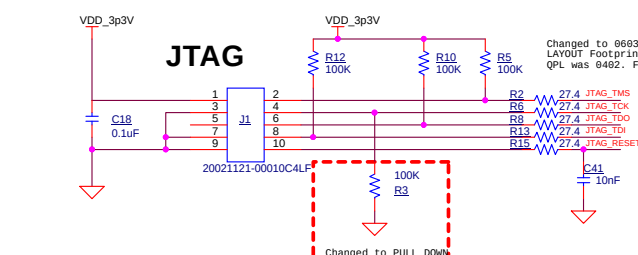
12V Going out the CAN J1-4 powers the User Interface Module



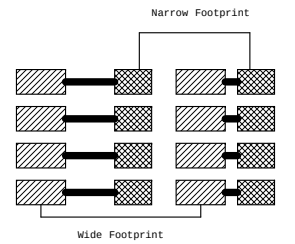
CAN COMMUNICATIONS



RS-232 SERIAL PORT

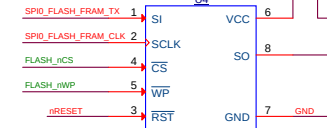


NARROW / WIDE footprints.



SPI0

FLASH

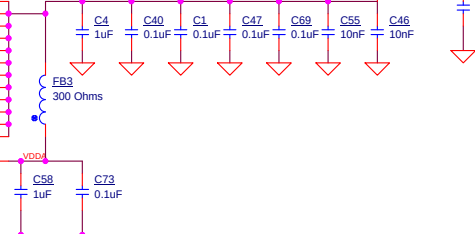


NON - POP

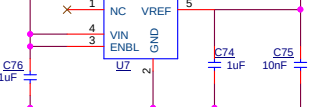
BOARD REVISION BIT DECODER:

BIT	2	1	0	
REV 0	0	0	0	MULE BOARD
REV 1	0	0	1	P1.5
REV 2	0	1	0	1218382 BOARD
REV 3	0	1	1	

Decoupling Capacitors for the Micro.

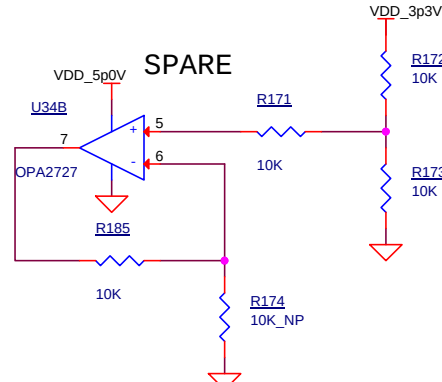
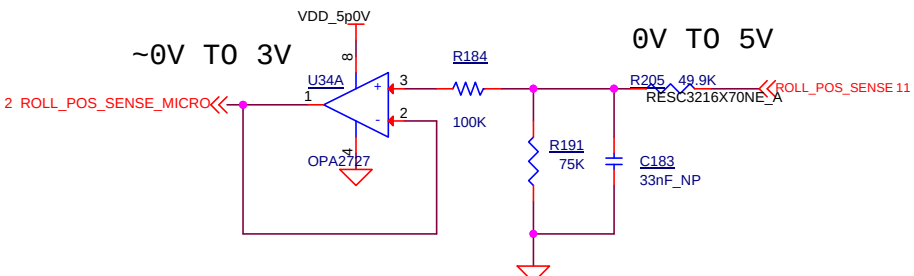
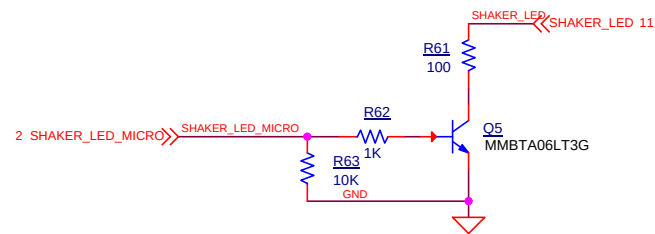
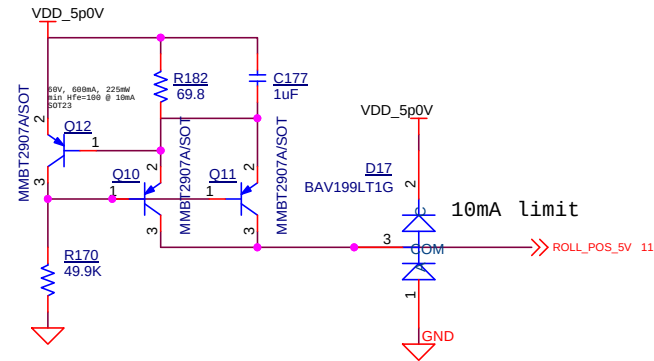
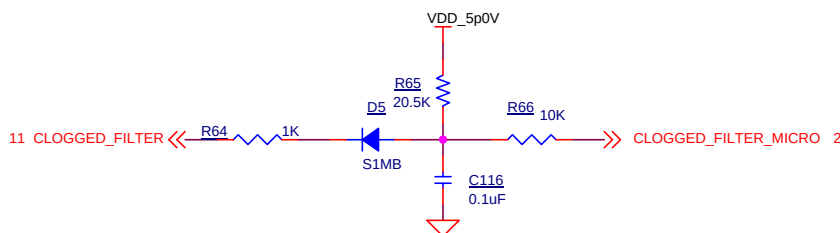
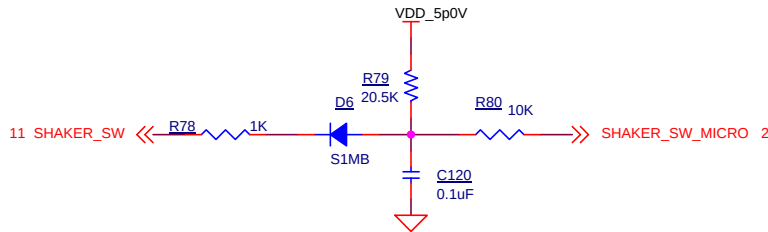
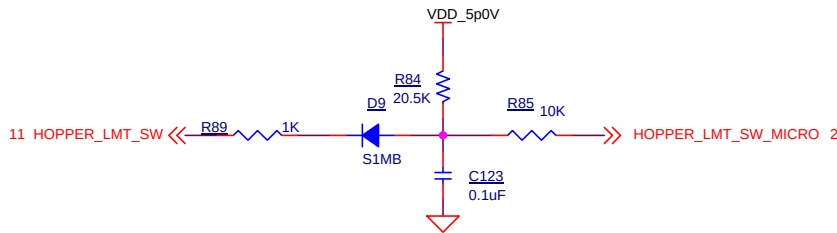
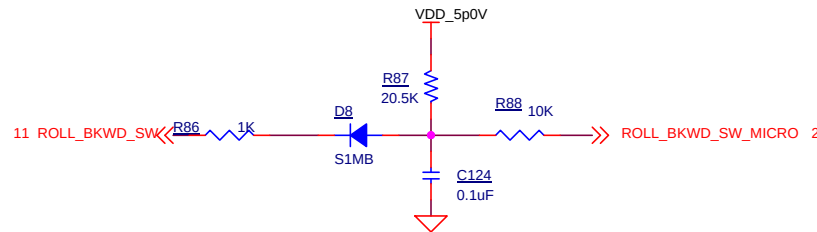
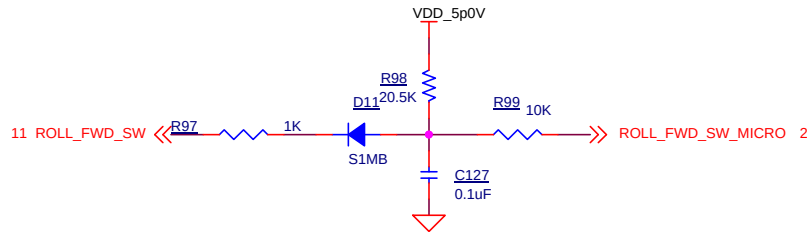
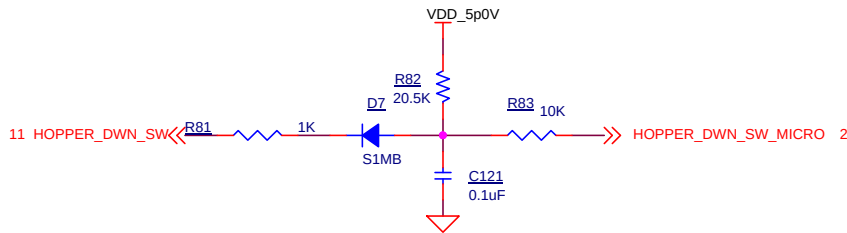
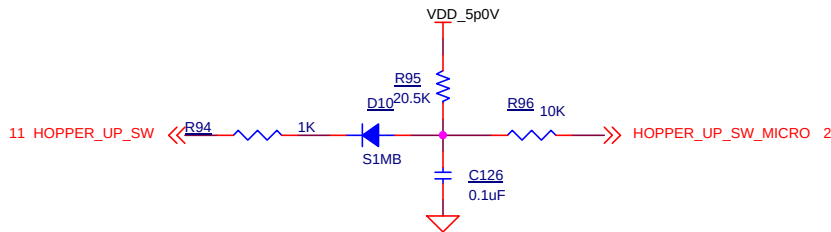
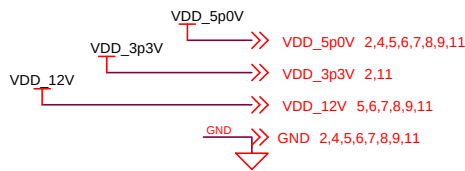


VDD_5p0V 3.0V Reference for A/D



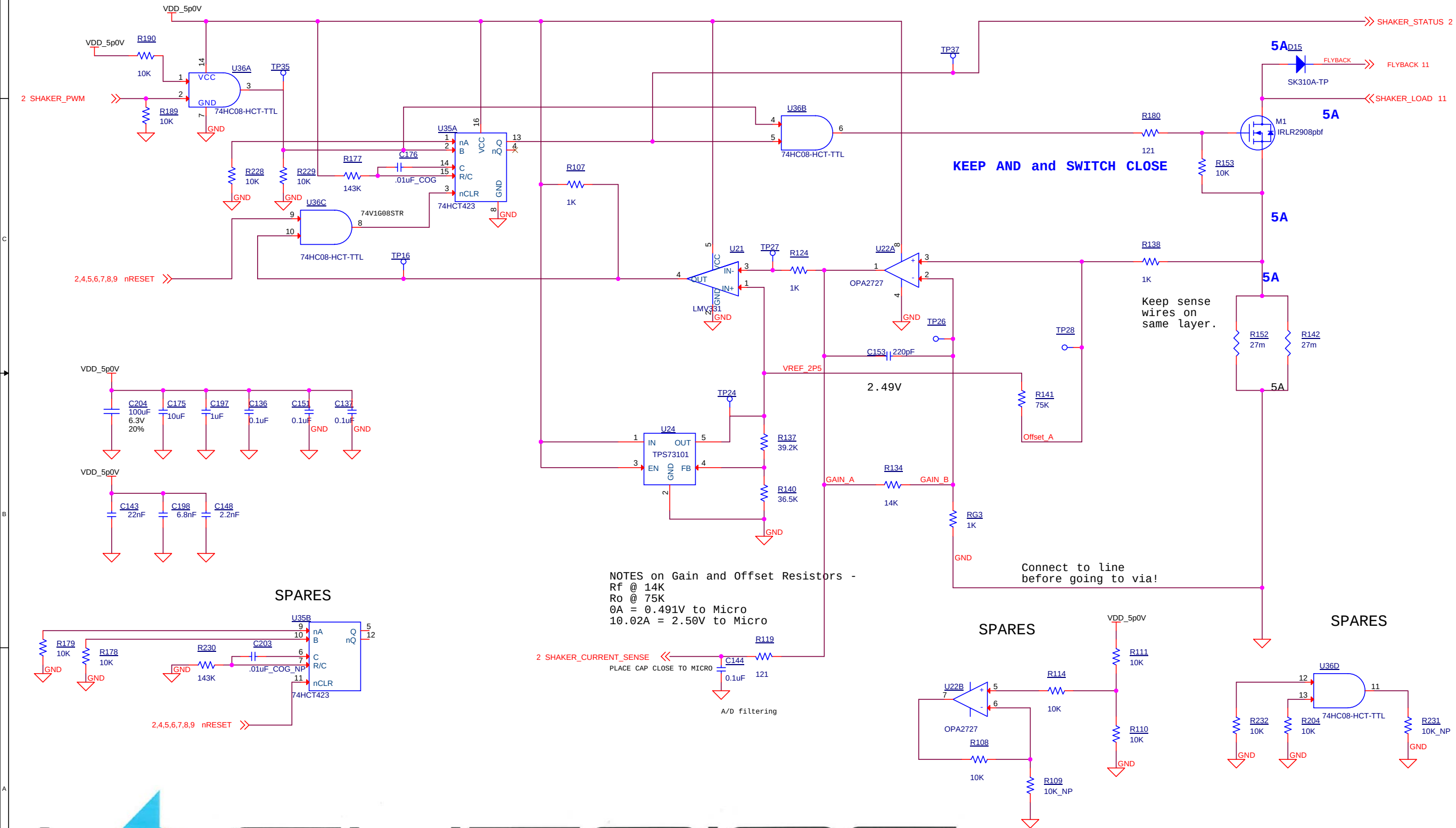
LIGHTNING

MAIN SWEEP BOARD INPUTS



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LIGHTNING MAIN SWEEP BOARD LSDPWM SHAKER

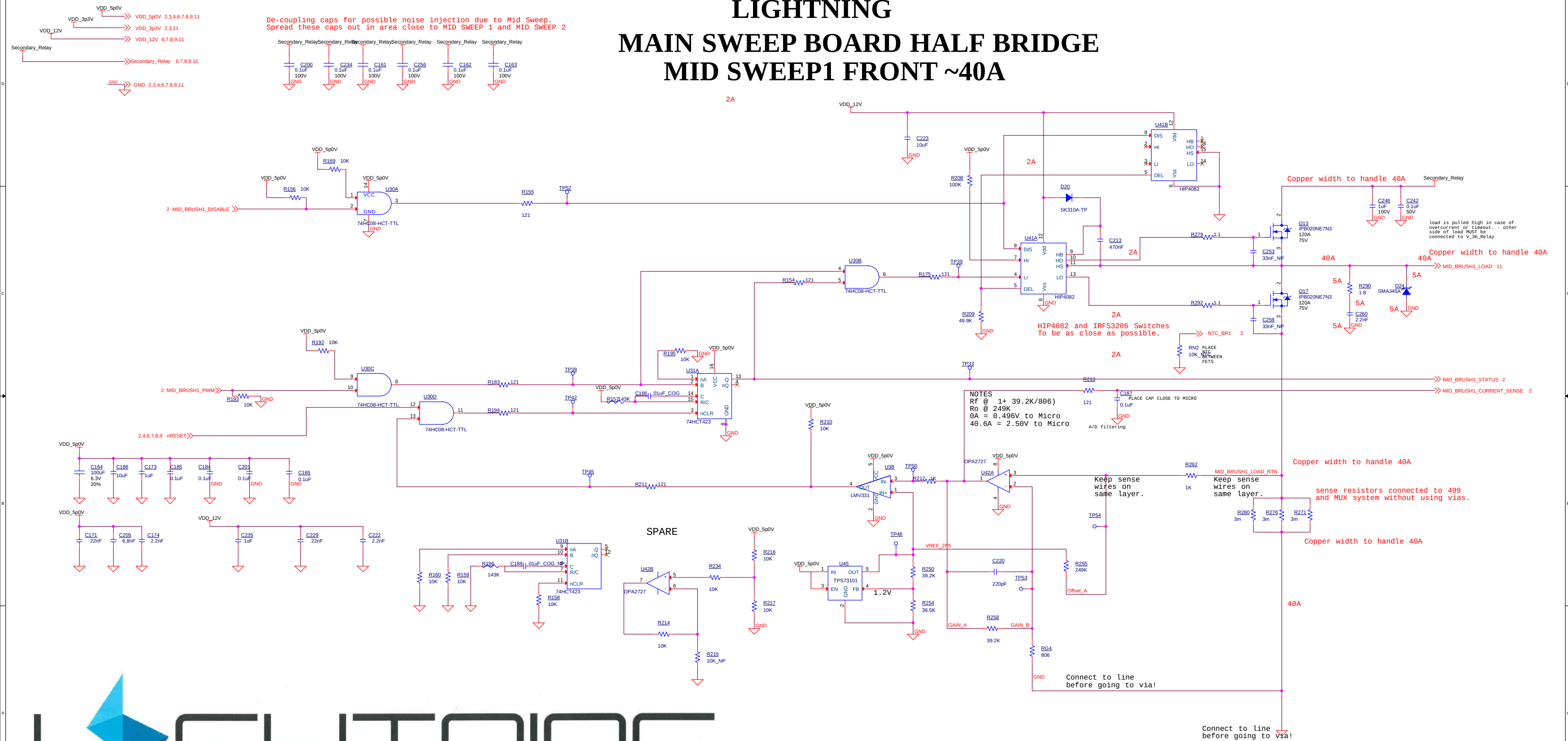


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LIGHTNING

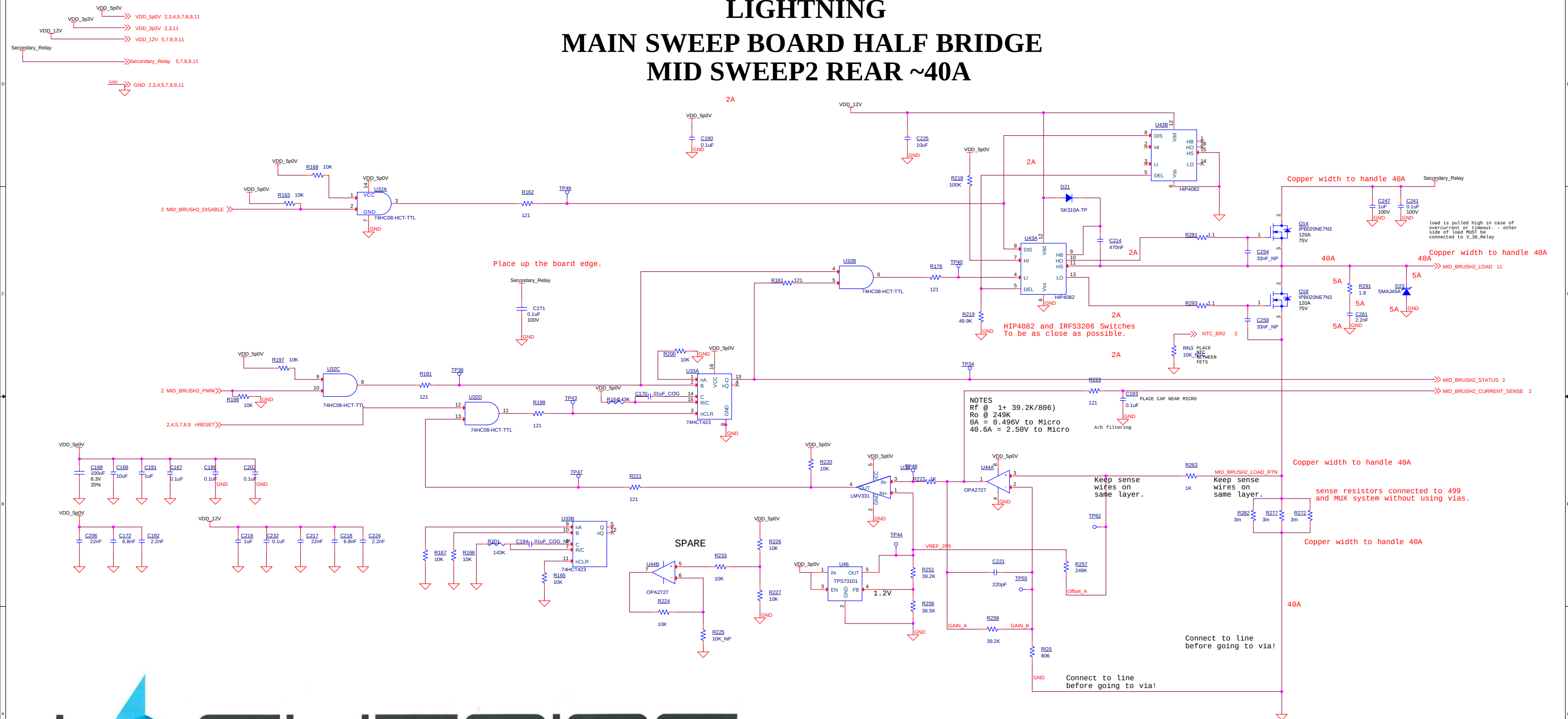
MAIN SWEEP BOARD HALF BRIDGE

MID SWEEP1 FRONT ~40A



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LIGHTNING
MAIN SWEEP BOARD HALF BRIDGE
MID SWEEP2 REAR ~40A

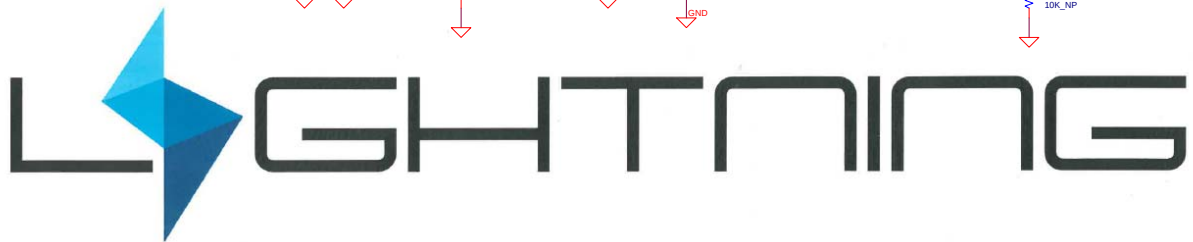
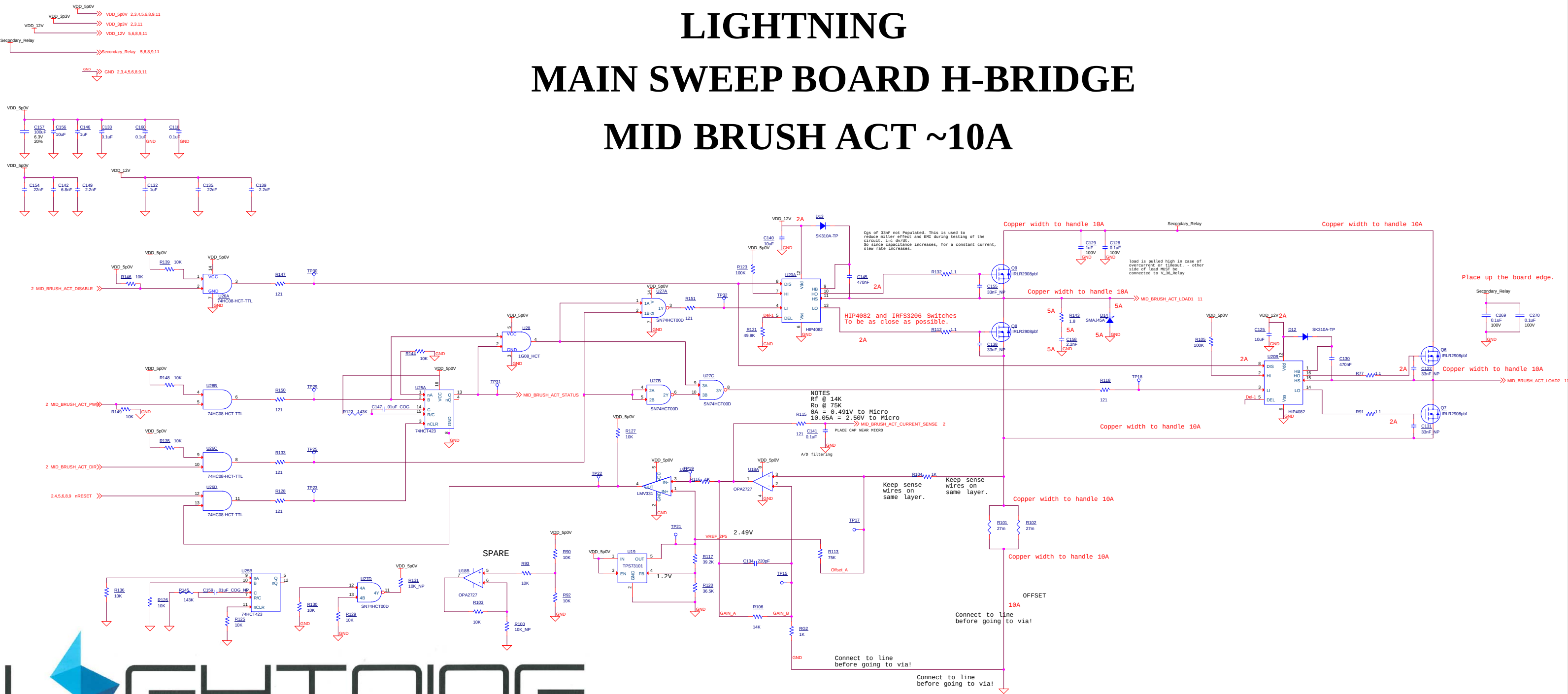


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LIGHTNING

MAIN SWEEP BOARD H-BRIDGE

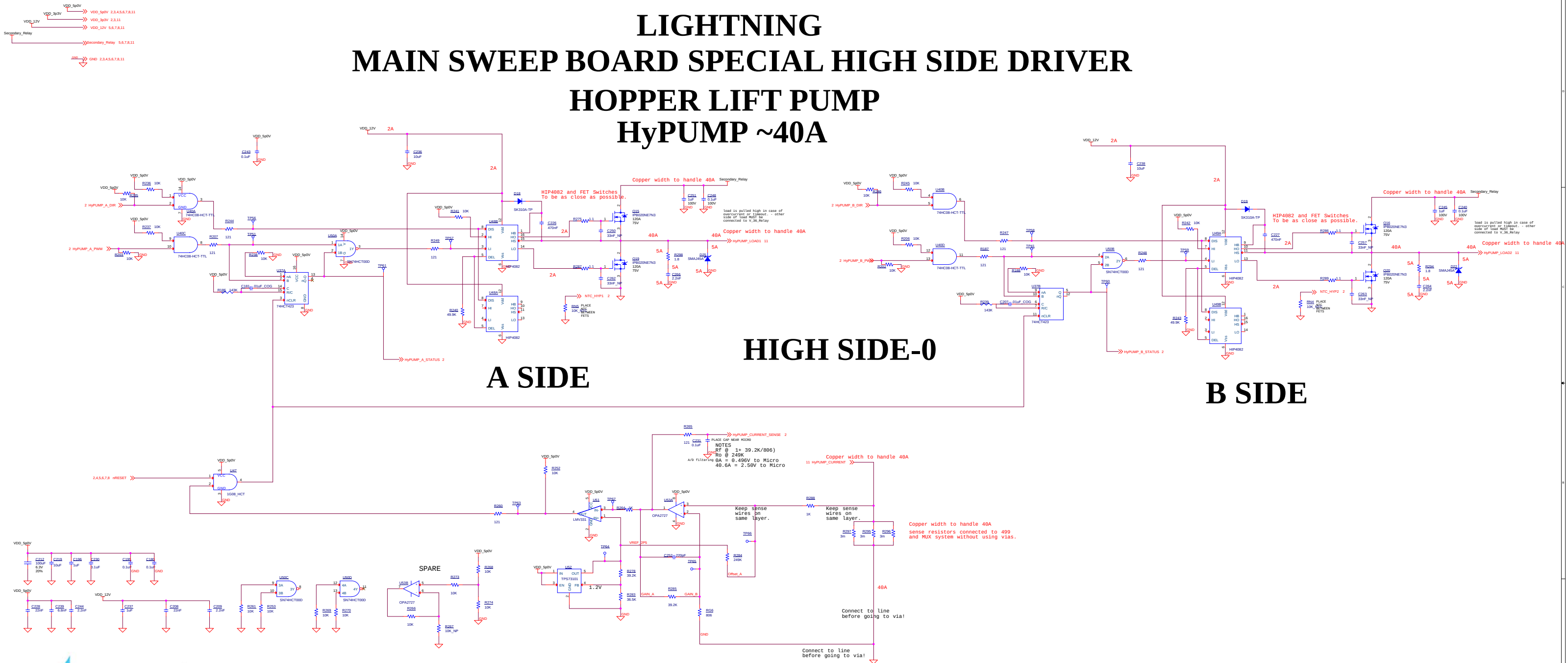
MID BRUSH ACT ~10A



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HOPPER ROLL ACT ~10A

LIGHTNING
MAIN SWEEP BOARD SPECIAL HIGH SIDE DRIVER
HOPPER LIFT PUMP
HyPUMP ~40A



LIGHTNING
MAIN SWEEP BOARD PRE-CHARGE
REMOVED AND PLACED ON SIDE SWEEP

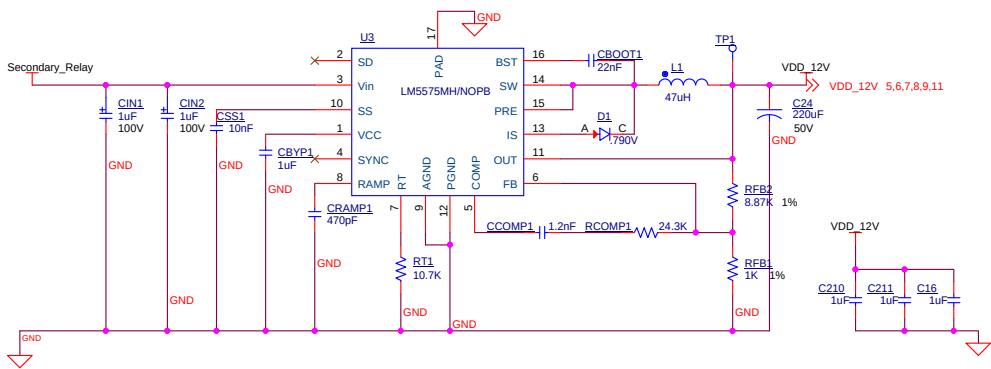


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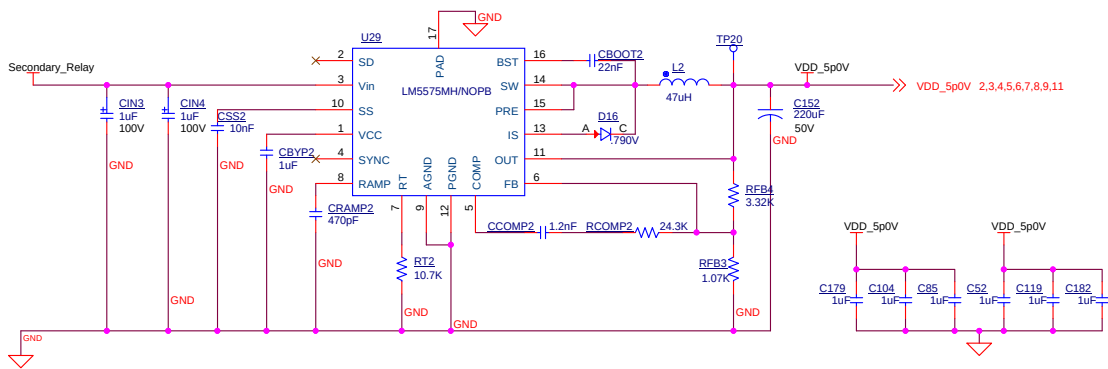
MAIN SWEEP BOARD: SUPPLIES and CONNECTORS

12V

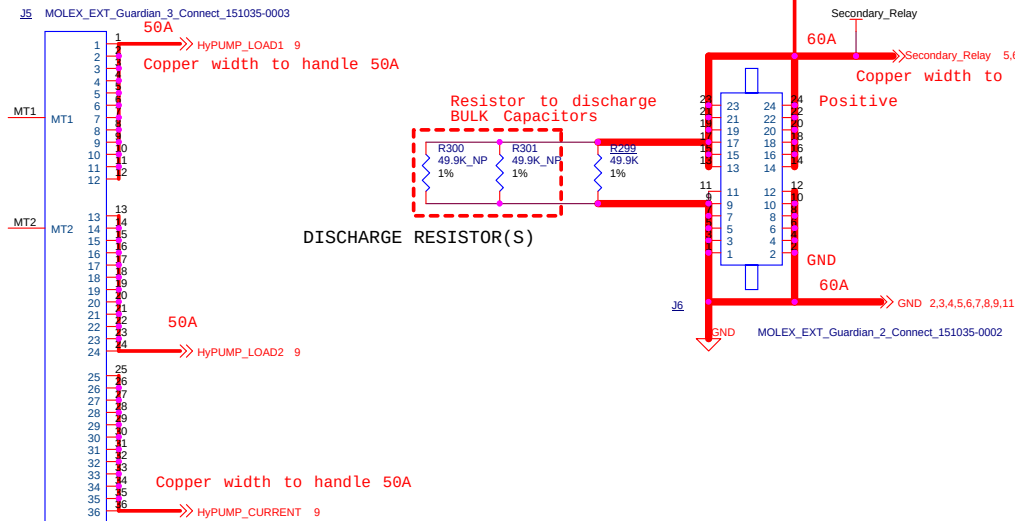
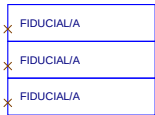
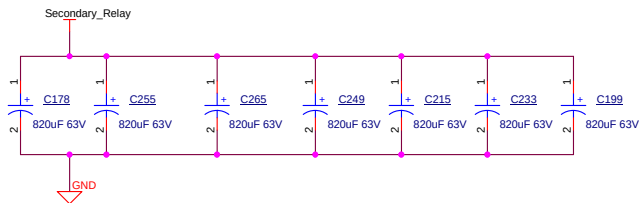
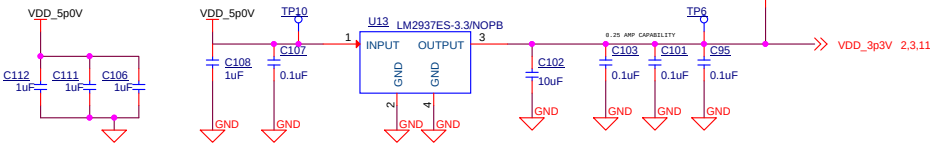


5V

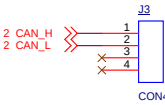
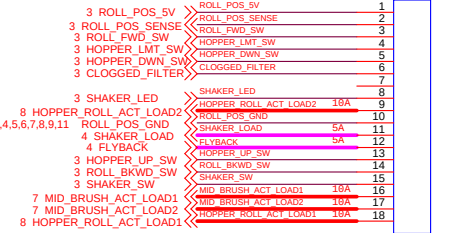
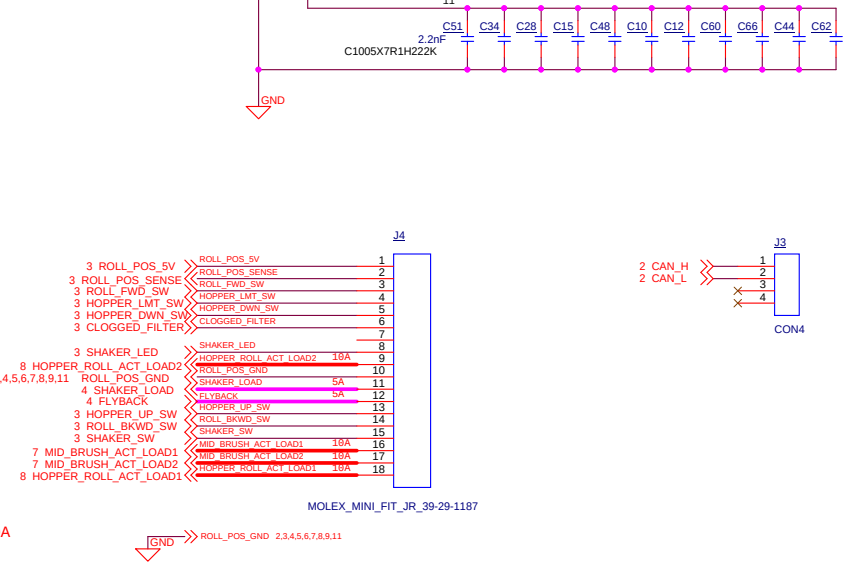
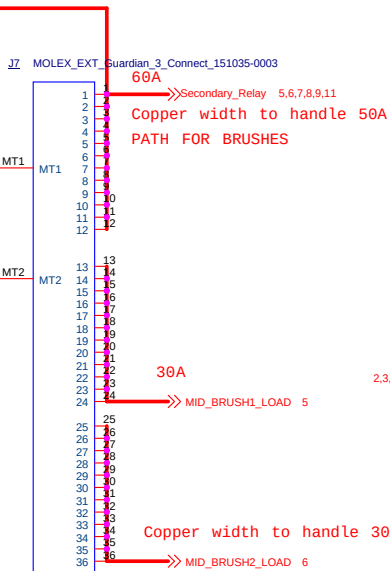
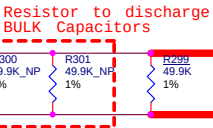
Need a bit more current than the linear can provide. Peaks of 2A.



3.3V



DISCHARGE RESISTOR(S)



LAYOUT NOTES - GENERAL NOTES

- 1) All nets to have vias to connect to for in circuit testing.
 - 2) Check Schematics for heavy RED wiring. There will be notes on current density.
- Rule of thumbs:
10-15mil per Amp on top level. (increase to reduce power dissipation if there is room)
40mil per Amp for inner traces.
Stack as needed to handle currents. Try to keep same size parallel between stacks.

LAYOUT NOTES - LSDPWM, HALF BRIDGES AND H-BRIDGES

- 1) Cu 250mils wide. ~ 10A capability. Need ~40A capability @ 1 oz Cu. May change for 2 oz Cu.
- 2) All Resistors at 1% Except 1Meg ohm Resistors can be 5% if no 1% available.
- 3) Current Sense resistors tied directly to 499 ohms on TOP LEVEL before via to ground. Connect Opamp Grounds to current sense Resistors on Top Level. USE MANY VIAS on node to ground after resistors and op-amps are connected.
- 4) To minimize ringing in the bootstrap circuit, keep the PCB traces from the HIP4082 to the external bootstrap capacitor and MOSFETs as short as possible. The bypass capacitor should be located as close as possible to the IC. Ceramic dielectric is the best choice for bypass and bootstrap capacitors.
- 5) Decoupling Caps added for 5V supply on each schematic that uses 5V & PWM and can add noise to it. Please keep these caps close to the circuitry in the page they are in.



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