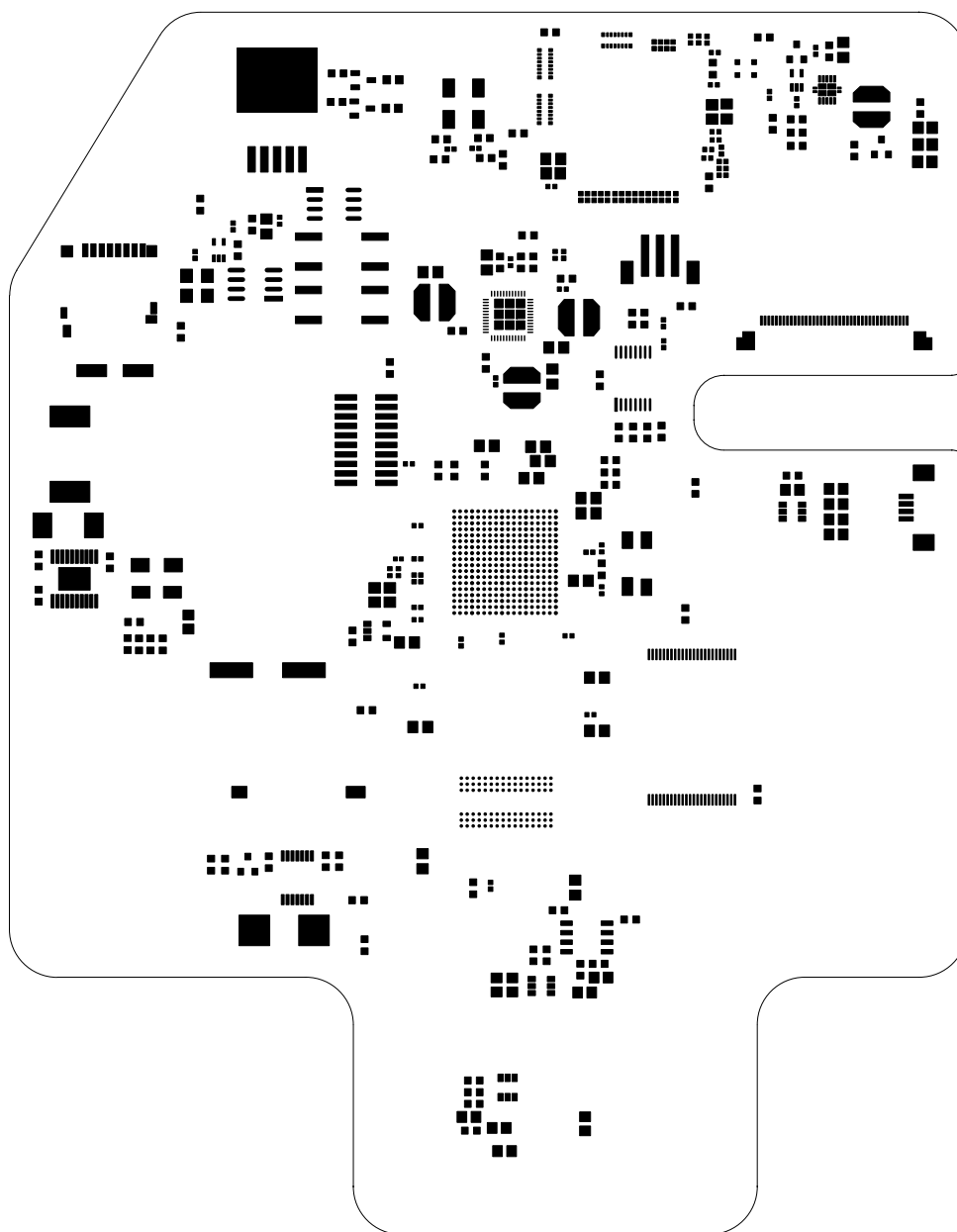
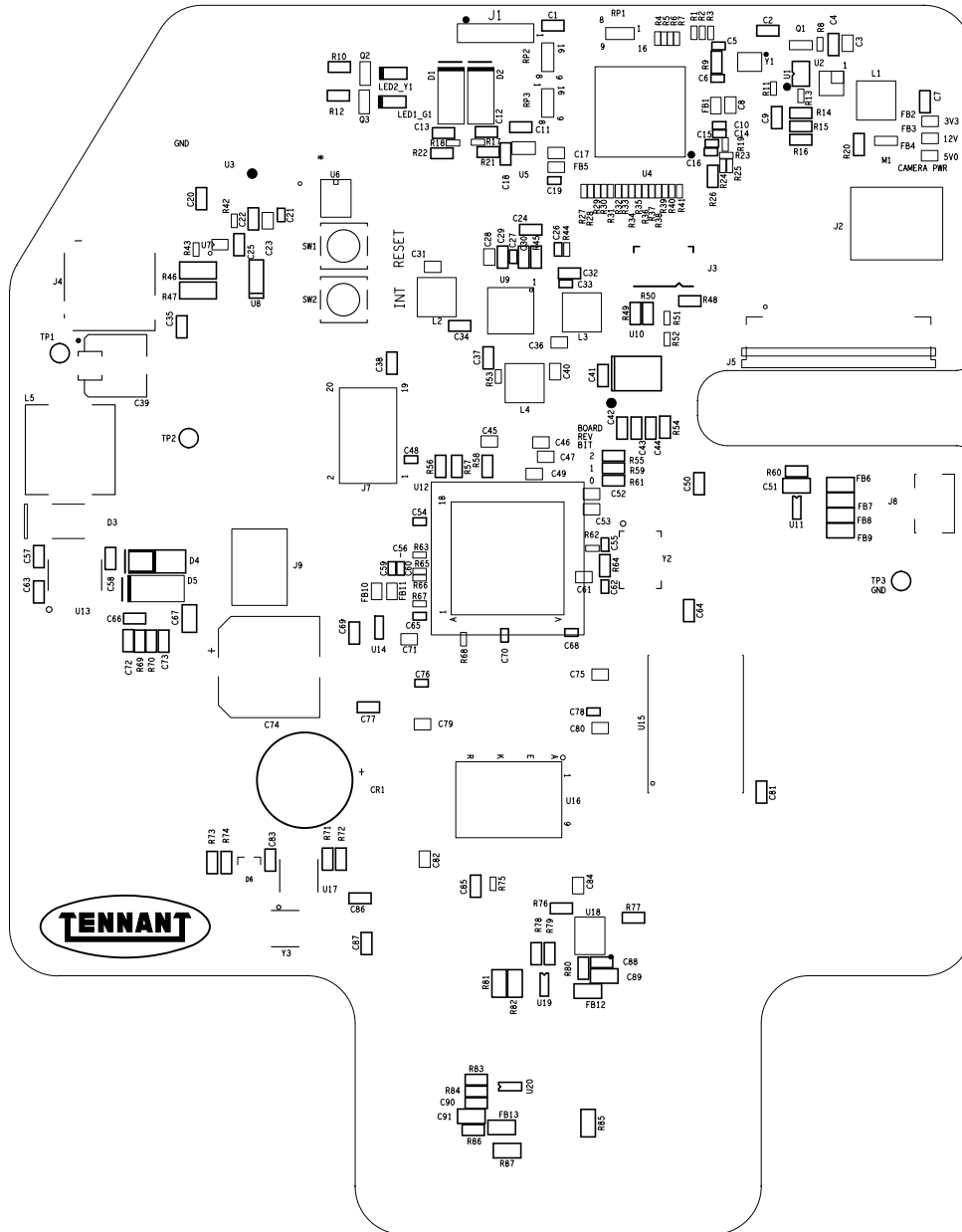


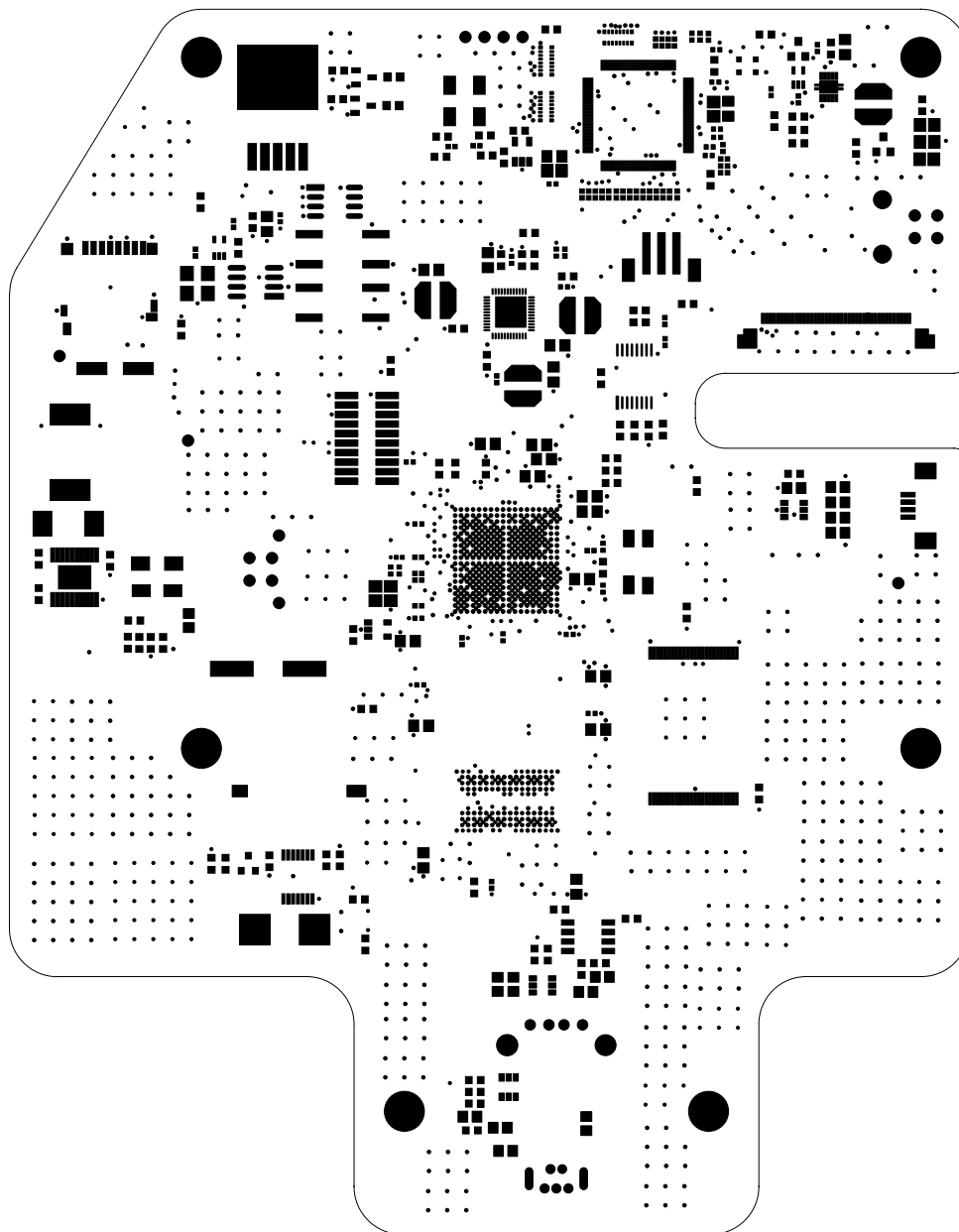
TENNANT CO Q25061-003GCP.ART SOLDERPASTE COMPONENT SIDE



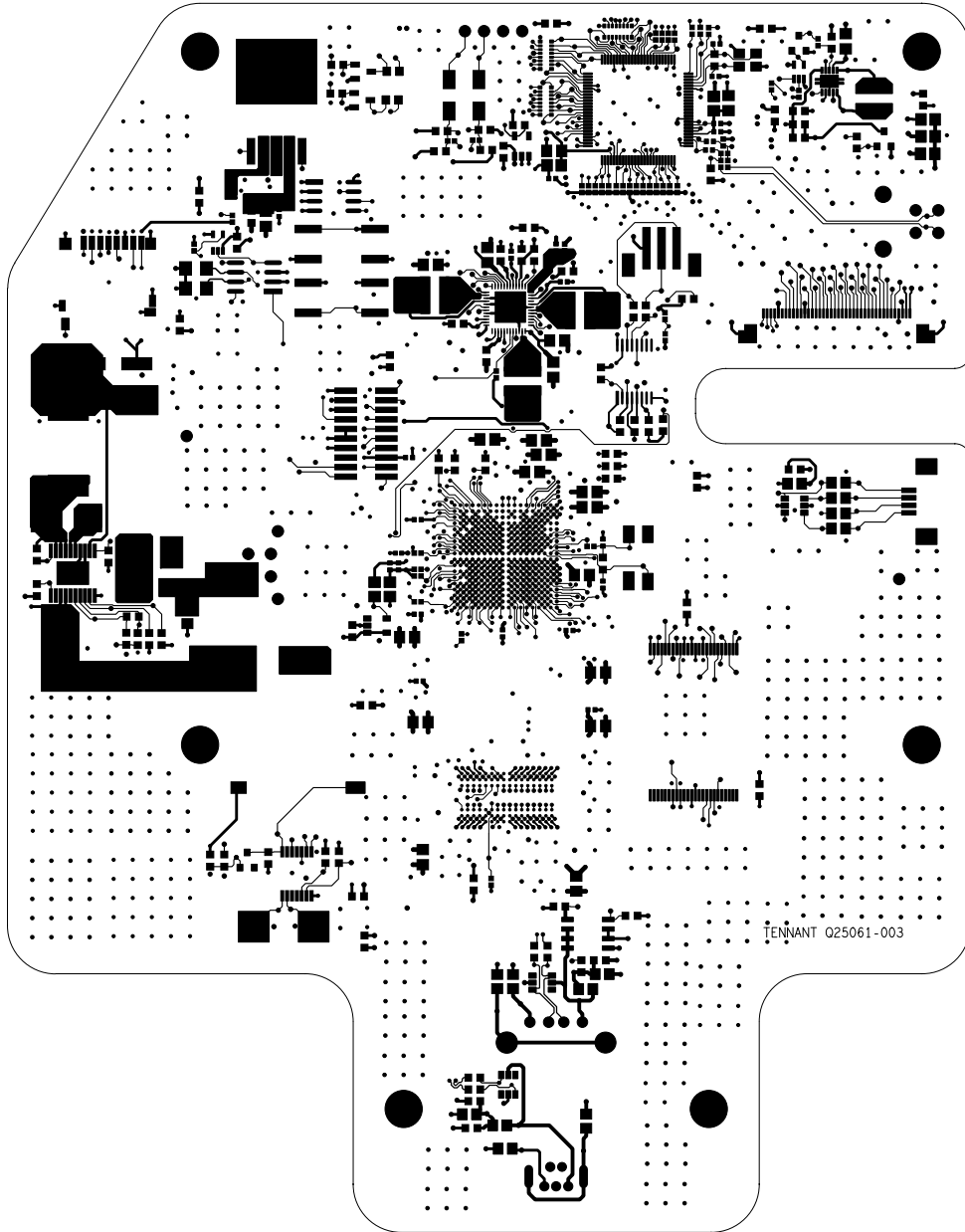
TENNANT CO Q25061-003GCS.ART SILKSCREEN COMPONENT SIDE



TENNANT CO Q25061-003GCM.ART SOLDERMASK COMPONENT SIDE



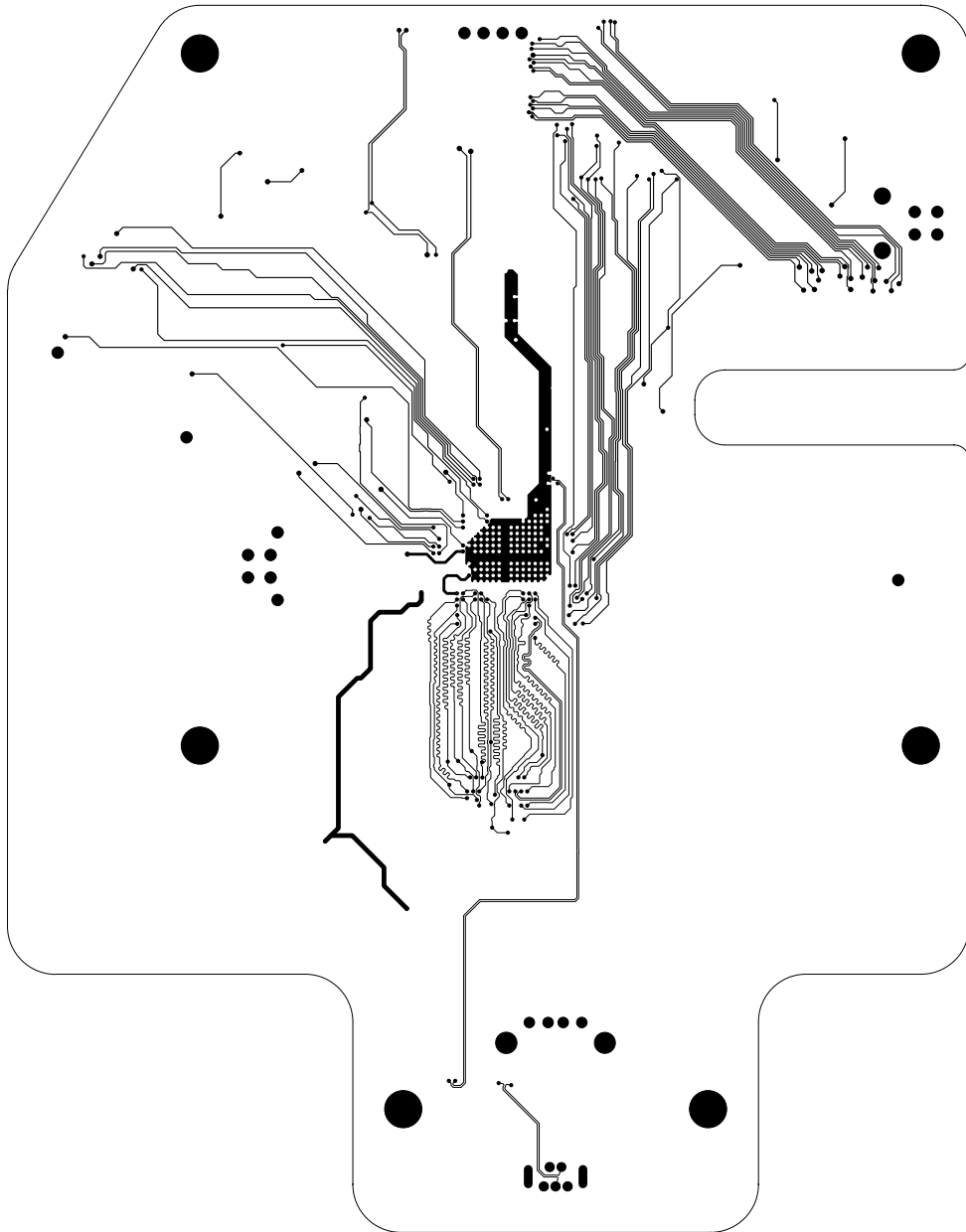
TENNANT CO Q25061-003G_C.ART COMPONENT SIDE LAYER 1



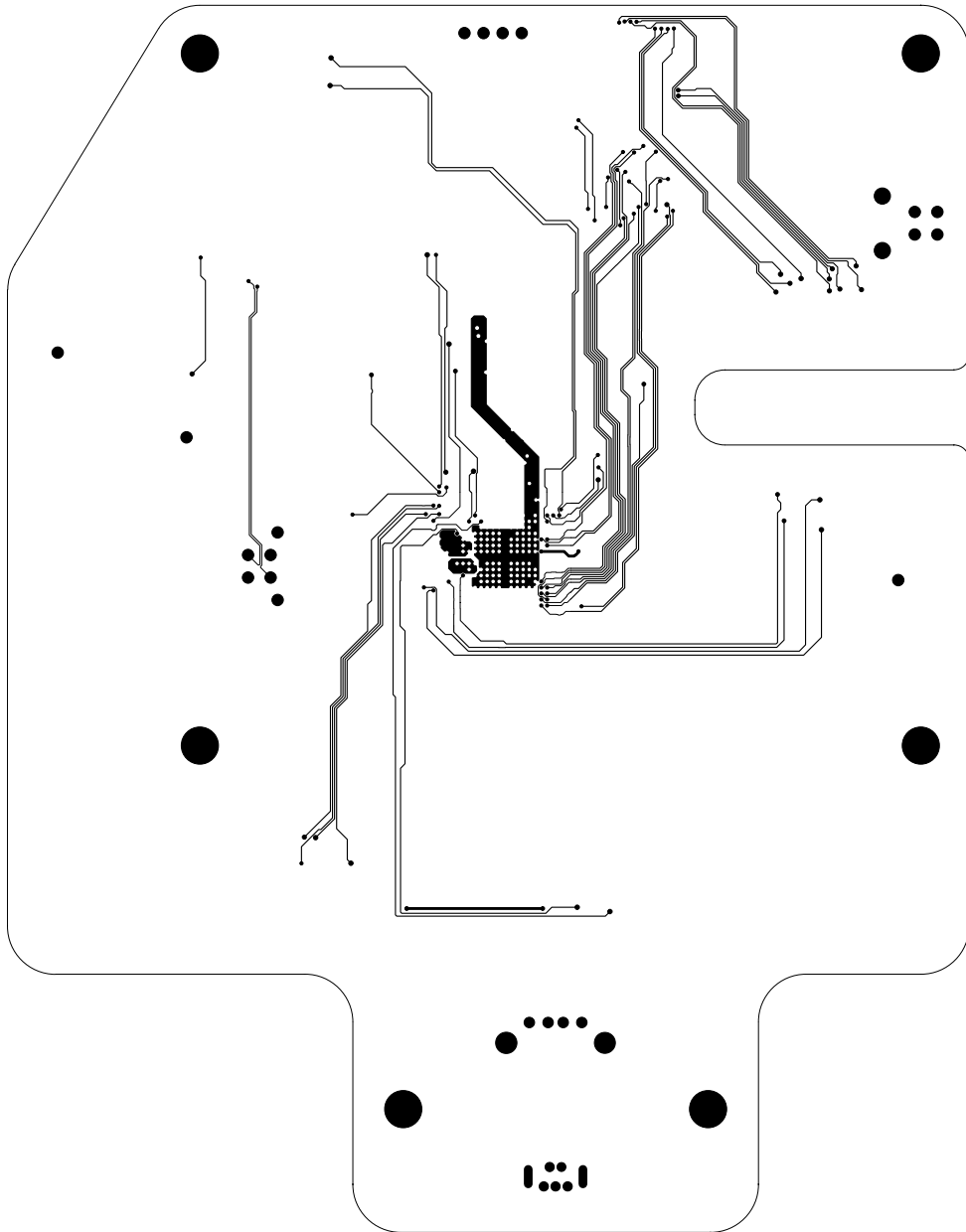
TENNANT CO Q25061-003GI1.ART GROUND PLANE LAYER 2



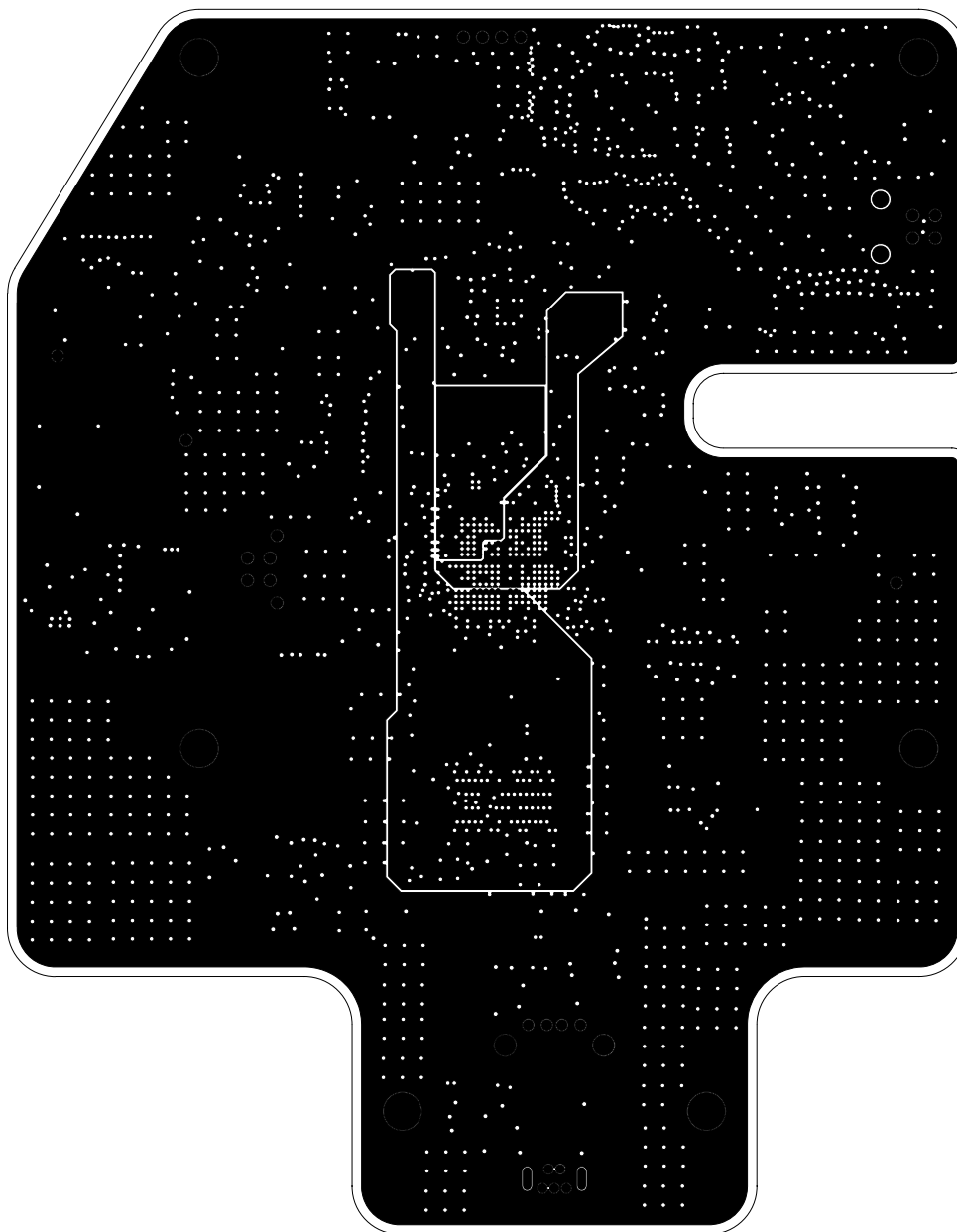
TENNANT CO Q25061-003GI2.ART SIGNAL - LAYER 3



TENNANT CO Q25061-003GI3.ART SIGNAL - LAYER 4



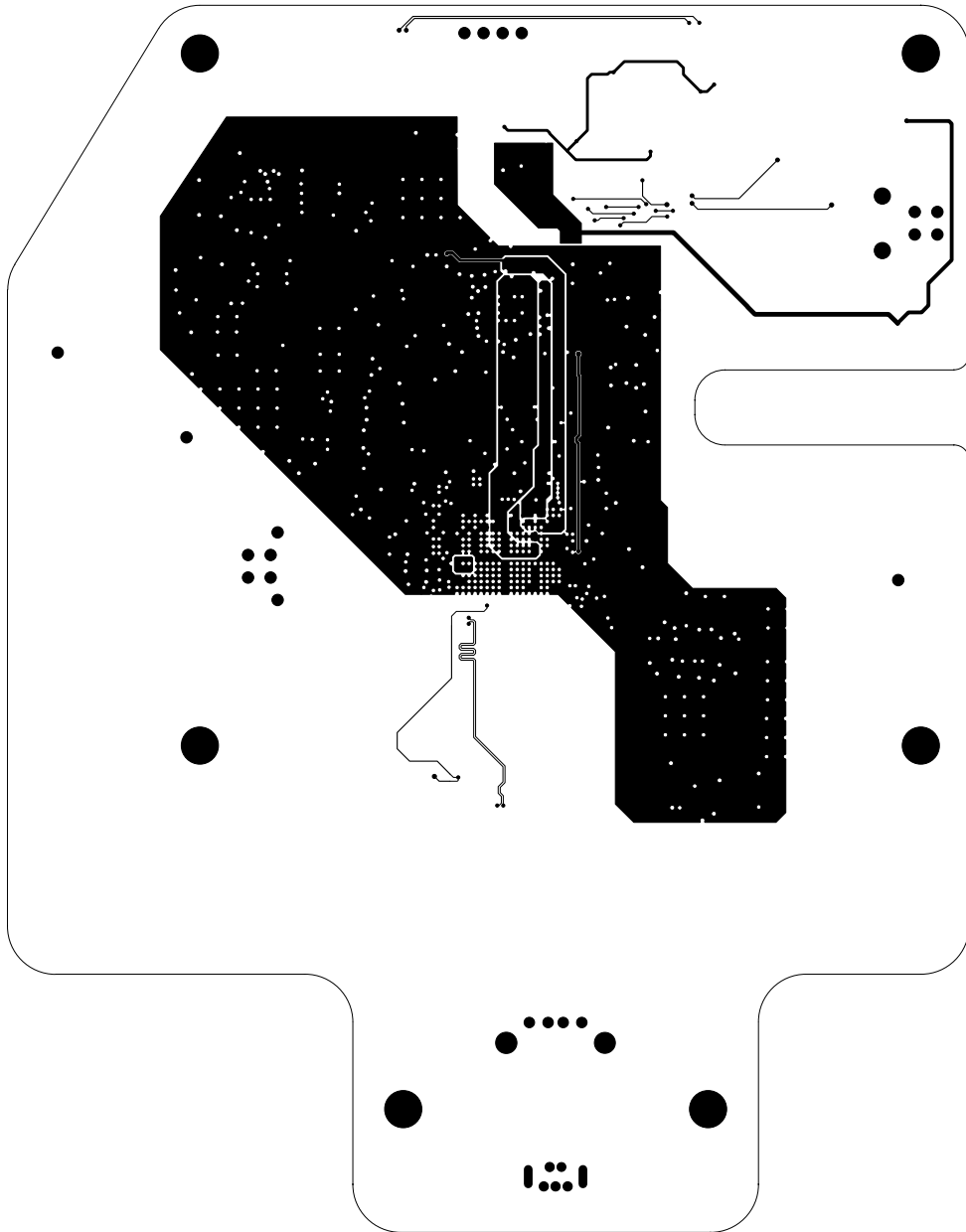
TENNANT CO Q25061-003GI4.ART POWER PLANE LAYER 5



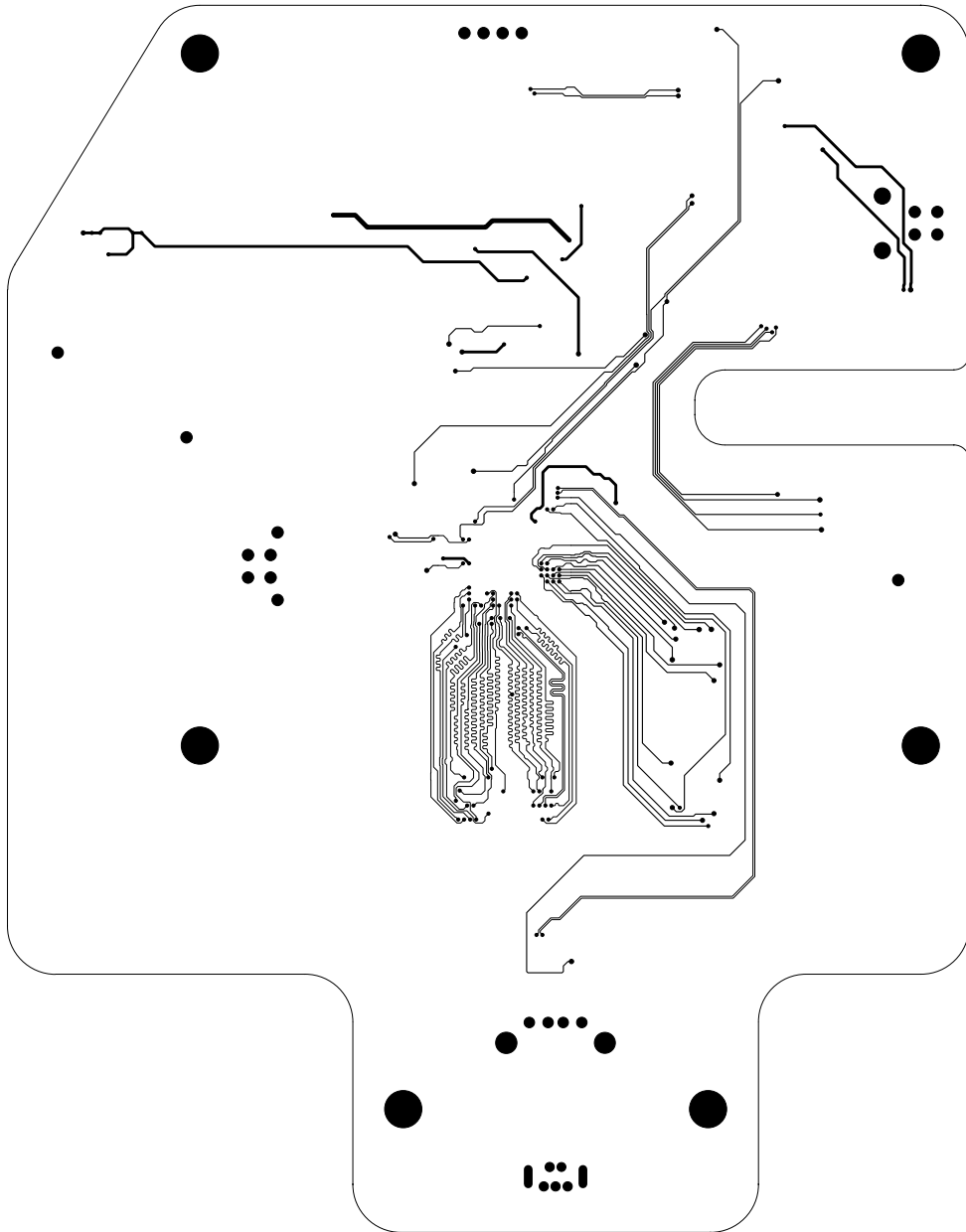
TENNANT CO Q25061-003GI5.ART GROUND PLANE LAYER 6



TENNANT CO Q25061-003GI6.ART SIGNAL - LAYER 7



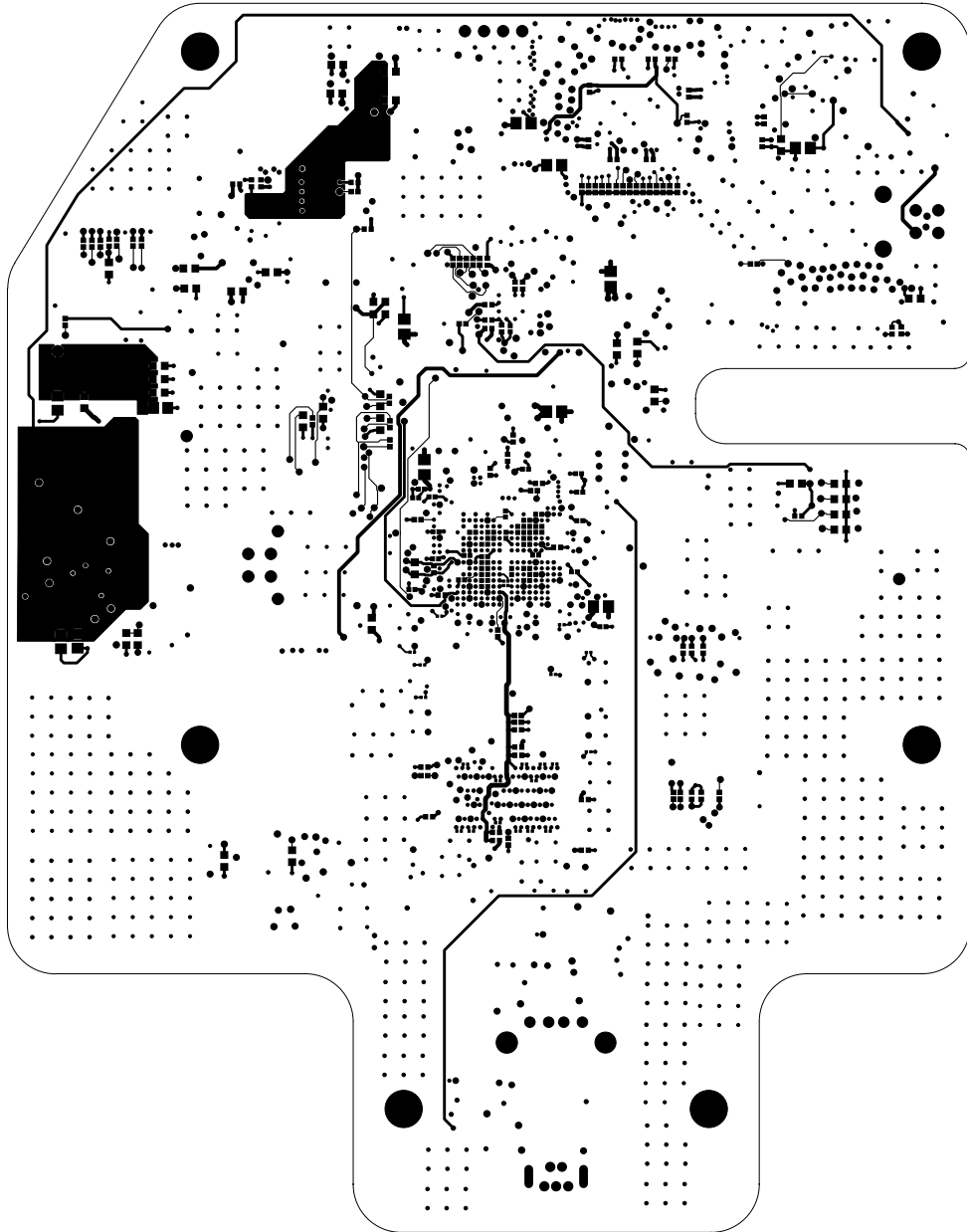
TENNANT CO Q25061-003GI7.ART SIGNAL - LAYER 8



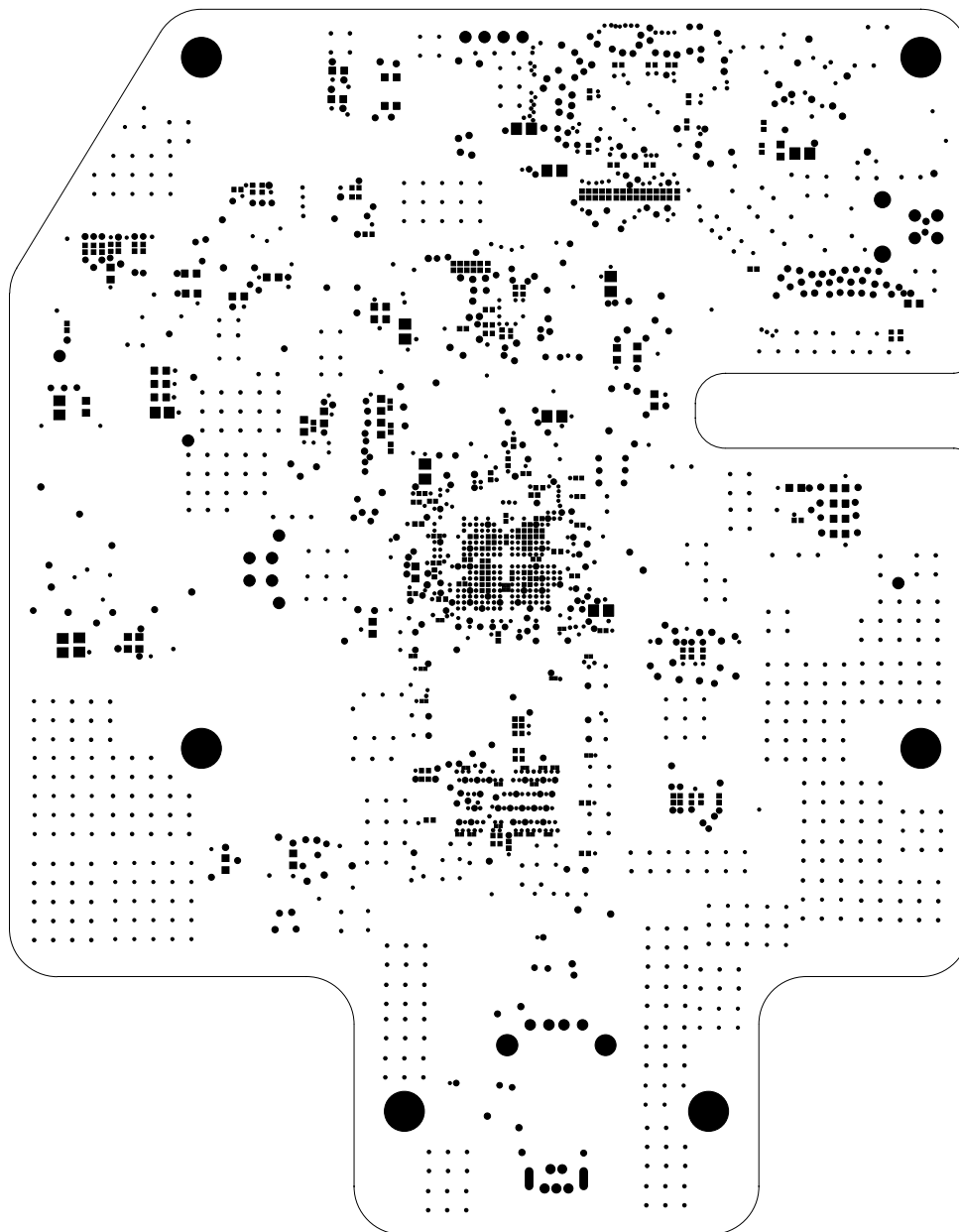
TENNANT CO Q25061-003GI8.ART GROUND PLANE LAYER 9



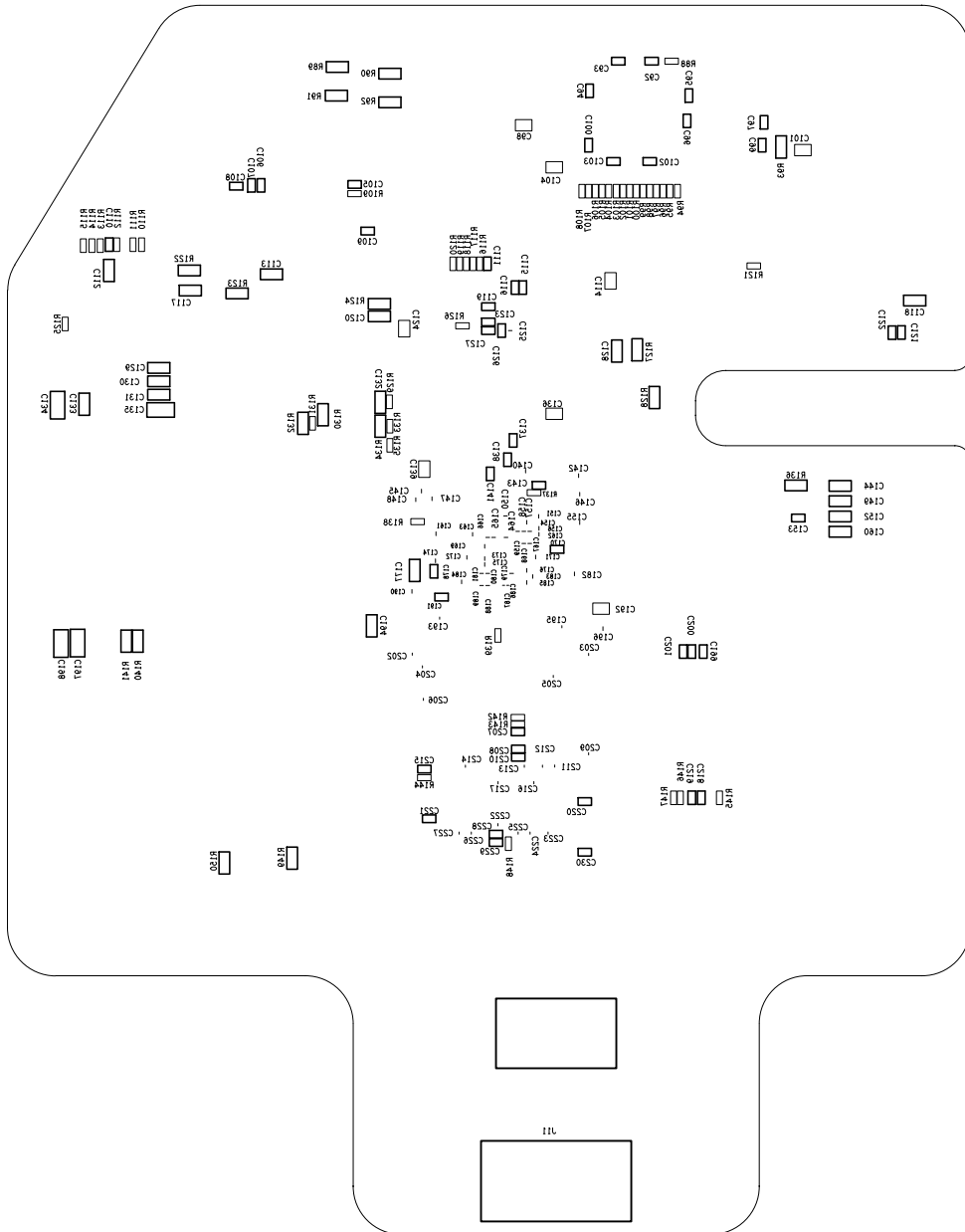
TENNANT CO Q25061-003G_S.ART SOLDER SIDE LAYER 10



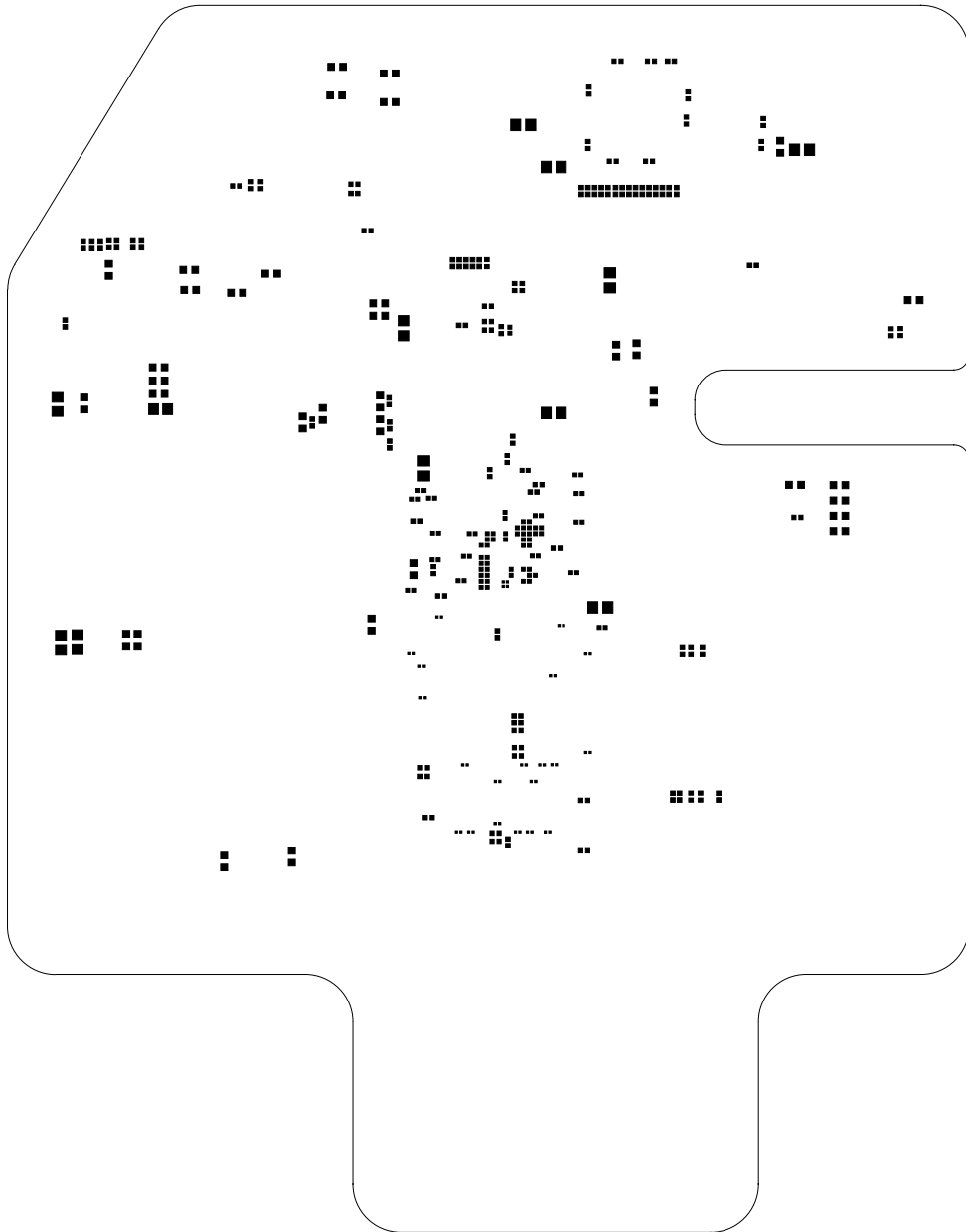
TENNANT CO Q25061-003GSM.ART SOLDERMASK SOLDER SIDE



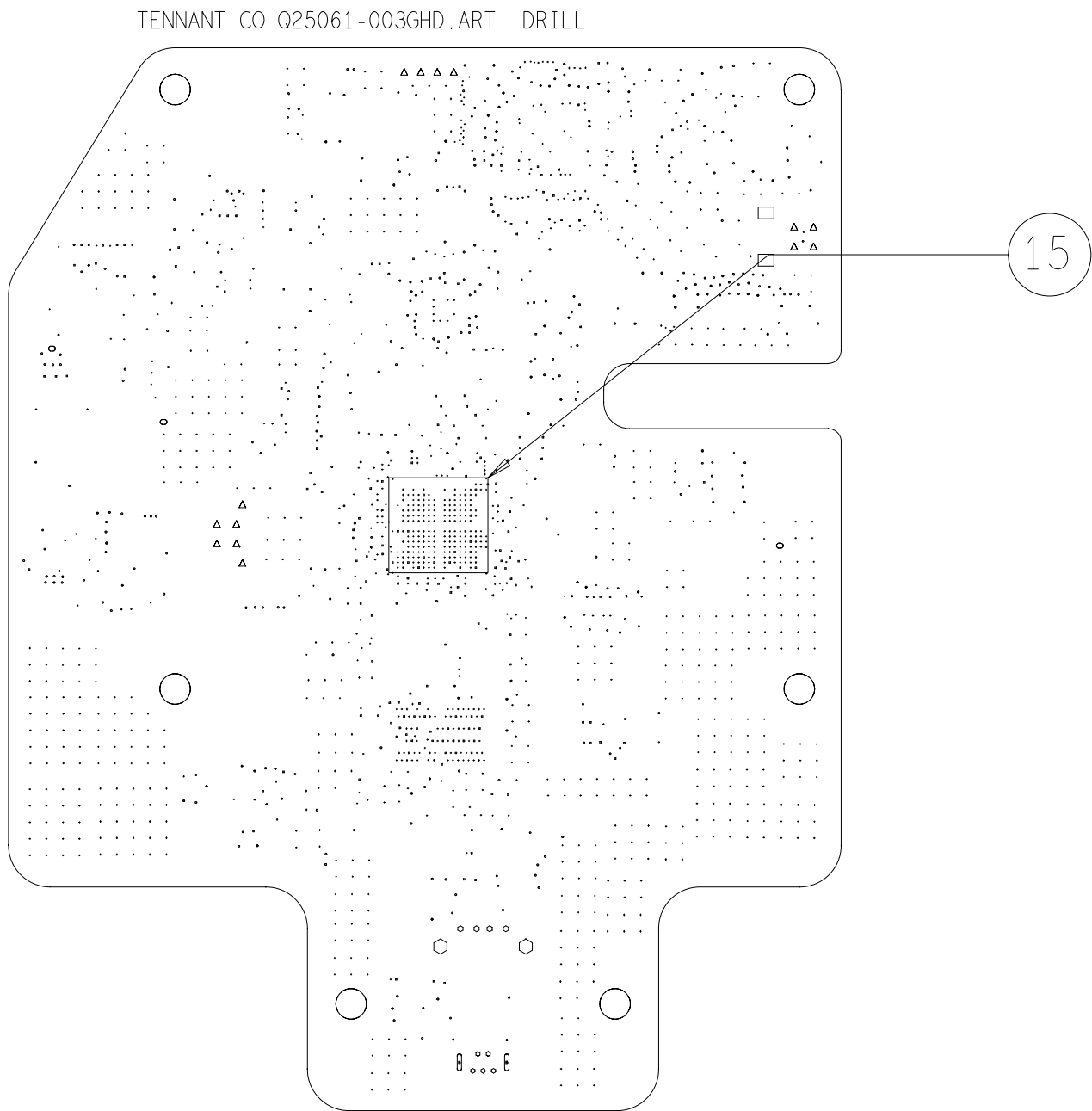
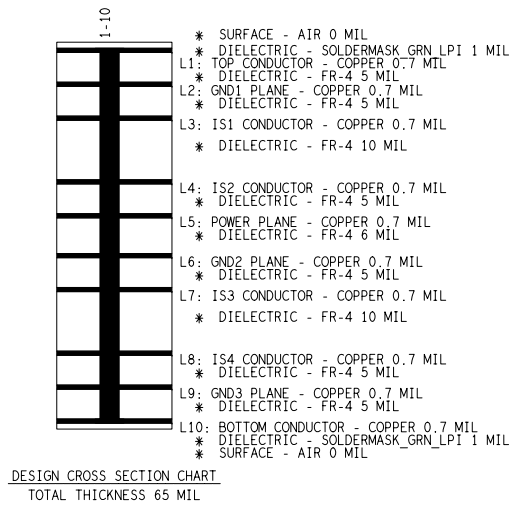
TENNANT CO Q25061-003GSS.ART SILKSCREEN SOLDER SIDE



TENNANT CO Q25061-003GSP.ART SOLDERPASTE SOLDER SIDE



| DRILL CHART: TOP to BOTTOM | | | | |
|----------------------------|------------|-----------|------------|------|
| ALL UNITS ARE IN MILS | | | | |
| FIGURE | SIZE | TOLERANCE | PLATED | QTY |
| · | 8.0 | +3.0/-3.0 | PLATED | 1196 |
| · | 8.0 | +3.0/-3.0 | PLATED | 236 |
| · | 10.0 | +3.0/-3.0 | PLATED | 164 |
| · | 10.0 | +3.0/-3.0 | PLATED | 246 |
| · | 10.0 | +3.0/-3.0 | PLATED | 4 |
| ° | 28.0 | +3.0/-3.0 | PLATED | 5 |
| ° | 36.0 | +3.0/-3.0 | PLATED | 4 |
| ° | 40.0 | +3.0/-3.0 | PLATED | 3 |
| ▲ | 40.0 | +3.0/-3.0 | PLATED | 14 |
| ○ | 91.0 | +3.0/-3.0 | PLATED | 2 |
| □ | 95.0 | +5.0/-5.0 | NON-PLATED | 2 |
| ○ | 185.0 | +5.0/-5.0 | NON-PLATED | 6 |
| ⌀ | 102.0x26.0 | +2.0/-2.0 | PLATED | 2 |



FABRICATION NOTES:

- 1.) MATERIAL SELECTION:
UL RECOGNIZED ZPMV2 MIN. 130C FLAME CLASS V-0 OR BETTER WITH A MINIMUM CTI RATING OF 175, .062 +/- 0.007 THICK. MATERIAL PER IPC-4101. SOLDERABLE SURFACES TO BE ENIG (ELECTROLESS NICKEL IMMERSION GOLD) FINISH. SEE CROSS SECTION FOR LAYER AND CONDUCTOR THICKNESSES - THIS IS AN IMPEDANCE CONTROLLED DESIGN.
- 2.) SOLDER RESIST: THE USE OF SOLDER RESIST COATING SHALL BE IN ACCORDANCE WITH THE REQUIREMENTS OF IPC-SM-840. ALL SOLDERABLE SURFACES ARE TO BE FREE OF SOLDER RESIST.
- 3.) SILKSCREEN: USE WHITE NON-CONDUCTIVE INK. ALL COMPONENT AND TESTPOINT LANDS ARE TO BE FREE OF INK.
- 4.) MANUFACTURER'S IDENTIFICATION: ADD IN ETCH OR TO SILKSCREEN.
- 5.) ELECTRICAL BARE BOARD TEST REQUIRED.
- 6.) DRILL SIZES ARE FINISHED SIZE AFTER PLATING.
- 7.) FABRICATE TO MEET EU ROHS DIRECTIVE.
- 8.) PCB MUST HAVE UL 94V-0 AND CTI RATING MARKED ON ONE SIDE.
- 9.) MAX WARP AND TWIST NOT TO EXCEED 0.010 PER LINEAR INCH.
- 10.) MIN ANNULAR RING: 0.003. MIN PLATED HOLE WALL THICKNESS 0.001.
- 11.) DIMENSIONAL TOL: XX +/- 0.010. XXX +/- 0.005.
- 12.) FABRICATE IN ACCORDANCE WITH IPC-600 OR IPC-6012 LATEST REVISION, CLASS 2.
- 13.) COPPER THEIVING OF THE SIGNAL LAYERS IS ALLOWED; SPACING TO ANY EXISTING BOARD FEATURE TO BE 0.060 MINIMUM.
- 14.) THIS IS AN IMPEDANCE CONTROLLED DESIGN. MATERIAL THICKNESSES, TRACE WIDTHS AND SPACINGS TO BE ADJUSTED TO ACHIEVE THE SPECIFIED DIFFERENTIAL IMPEDANCE:

60 OHM SINGLE ENDED IMPEDANCE:
INTERNAL LAYERS: .004" TRACE WIDTH
EXTERNAL LAYERS: .0051" TRACE WIDTH

90 OHM DIFFERENTIAL IMPEDANCE:
INTERNAL LAYERS: .0047" TRACE / .005" SPACE
EXTERNAL LAYERS: .007" TRACE / .006" SPACE

100 OHM DIFFERENTIAL IMPEDANCE:
INTERNAL LAYERS: .004" TRACE / .0062" SPACE
EXTERNAL LAYERS: .0051" TRACE / .006" SPACE
- 15.) ALL .008 DIAMETER HOLES IN NOTED AREA TO BE PLUGGED FROM THE TOP SIDE (LAYER 1 SIDE) WITH EITHER UV OR THERMALLY CURED PLUGGING MATERIAL. THE PLUGGING MATERIAL SHALL NOT DRIP OUT THE BOTTOM OF THE PCB.

TENNANT CO Q25061-003GAT.ART ASSEMBLY TOP

