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1 Scope and Purpose

This specification defines the minimum acceptable requirements applicable to the fabrication of printed circuit boards for Benchmark Electronics. Compliance to this specification is mandatory unless BEI provides a written waiver. The purpose of this specification is to address manufacturing requirements for BEI and should be used as a supplement to the specifications called out on the supplied fabrication drawings.

In the event that the end customer (BEI's customer) has a particular specification that is more stringent than this specification, then the end customer's specification shall be adhered to. If clarification of any item within this specification is required, contact BEI for further explanation. Unless otherwise specified, follow IPC-6012, Class 2 for all issues that are not covered within this specification or the end customer's specification.

This specification is intended to be used by printed circuit board fabricators, and BEI SDE, SQE and incoming inspectors.

2 References

- IPC-6012 Qualification and Performance Specification for Rigid Printed Boards.
- IPC-A-600 Acceptability of Printed Circuit Boards
- IPC-9252 Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards

IPC-TM-650	Test Methods
IPC-7721	Repair and Modification of Printed Boards and Electronic Assemblies
IPC-SM-840	Qualification and Performance of Permanent Solder Mask
IPC-4552	Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Circuit Boards
IPC-4553	Specification for Immersion Silver Plating for Printed Circuit Boards
IPC-4554	Specification for Immersion Tin Plating for Printed Circuit Boards
J-STD-020	Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
J-STD-033	Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices
J-STD-609	Marking and Labeling of Components, PCBs and PCBA's to Identify Lead (Pb), Pb-Free and Other Attributes
IPC-4101	Specifications for Base Materials for Rigid and Multilayer Printed Boards
UL 796	Recognized Component Index
IPC-1752	Materials Declaration Management

3 Definitions

Automated Optical Inspection (AOI): camera-based method to perform visual inspection

Certificate of Compliance (C of C): document specifying that a lot of delivered product meets requirements.

Diameter True Position (DTP): a measure of the hole position accuracy on a PCB.

Electroless Nickel/Immersion Gold Plating (ENIG): surface finish commonly used on printed circuit boards.

Hot Air Solder Level (HASL): surface finish commonly used on printed circuit boards.

Immersion Silver (IAG): surface finish commonly used on printed circuit boards.

Organic Solderability Preservative (OSP): surface coating applied to printed circuit boards.

Supplier Development Engineering (SDE): function responsible for driving improvement activities with our suppliers.

Supplier Quality Engineer (SQE): individual responsible for setting requirements for vendors and measuring compliance to these requirements.

4 Requirements

The following order of documents takes precedence:

- a) Purchase Order (PO)
- b) Part Specific Electronic Data Base
- c) Part Specific PCB Fabrication Drawing including panel drawing as required
- d) OEM Customer's Specification
- e) Compliance to this document (BE-46003)
- f) PCBs shall conform to the requirements of IPC-6012 Class 2 and acceptability of companion document IPC-A-600 Class 2.
- g) Business contracts provided that they do not deviate from the compliance to the above documents

PCB suppliers need to follow requirements of this document. Compliance verification to this document may include:

- supplier audit,
- incoming inspection of bare boards, or
- BEI review of supplier C of C through certificate verification. This is usually accomplished by repeating select measurements while following IPC-TM-650 methods.

Benchmark groups acting as SCA, SDE, SQE, and Purchasing agents are responsible for providing this document to PCB suppliers.

The Supplier is responsible for correct photo tool and fabrication database generation from the supplied part specific database without plot approvals from BEI.

It is the Suppliers' responsibility to ensure that the revisions on the BEI purchase order match the revisions on the BEI part specific PCB fabrication drawings and electronic database.

It is the Suppliers' responsibility to run a complete Design Rules check on the supplied Electronic data to identify potential violations, and to compare this data to the supplied part specific drawings to review for potential discrepancies. If the artwork is modified the supplier shall compare the changes to the source data to make sure that the design has not been violated. The Supplier shall communicate any discrepancies or requests for deviation to BEI, in writing, prior to fabricating the boards.

Problems and deviations that are discovered during the manufacturing process will be handled by placing the parts ON Hold until the question is resolved or by a Pre Delivery Variance request before the finished parts are shipped.

Once a part has been manufactured by the supplier using a particular series of process steps and qualified and accepted at BEI the process steps shall not be changed. This does not apply to bath change-outs and corrections that are part of routine operations. If the process is changed to a different chemical makeup or a different vendor, the manufacturing process may need to be requalified at BEI's discretion before more boards are accepted.

No X-outs are allowed on panelized boards without prior written authorization from Purchasing / SCA and SDE. The number of X-outs per panelization will be specified on the drawing showing the layout of the array or separate specification sheet when necessary. When authorized, the scrap boards shall have an "X" marked on both sides with permanent black ink. X-outs must be packaged separately and labeled. Panels that have defects which make all parts on the panel suspect shall be discarded rather than being Xed out. Examples of this type of defect include voids, delamination, peeling copper, and soldermask cracking.

BEI will not accept boards with less than 50% of expected shelf life remaining as determined by board finish, unless pre- approved by SDE/SQE.

- 1 year shelf life: ENIG, Flash Gold, SN100CL (LF HASL), and PB HASL
- 6 month shelf life: OSP, Immersion Silver, and Immersion Tin

In cases where removing the old finish and applying a new finish is being considered:

- a) Approval prior to stripping finish is required,
- b) proper fabrication and storage requirements have been followed, and
- c) solderability test coupons and results shall be included with PCBs.

No portion of the manufacturing, testing or inspecting of any product for BEI may be sub-contracted to another supplier, without prior written authorization. This requirement does not include sub-contracted suppliers that perform tasks within the facility of the BEI supplier. (i.e. An in-house stores process)

The Supplier is responsible for ensuring that adequate process controls are in place to provide quality product to BEI. The supplier must make this data available to BEI upon written request.

5 PCB Laminate Construction

Exposed weave between conductors is not acceptable.

Warp and Twist: 70 microns per centimeter (7 mils per inch maximum). The maximum warp and twist shall not exceed 1.8 mm (70 mils) across the entire PCB regardless of width or length. The warp and twist in areas of array packages like BGAs and CGAs shall not exceed 30 microns per centimeter (3mils per inch).

- Bow and Twist shall be measured using IPC-TM-650 number 2.4.22.
- Delamination and Blister shall meet IPC-A-600 Class 2 (same as Class 3.)

Subsurface Imperfections and Foreign Inclusions: Subsurface imperfections shall be treated as Foreign Inclusions when determining acceptability per IPC 600 Class 2 (same as Class 3), with the following restrictions:

- Translucent imperfections cannot bridge conductors, and when located between conductors, the imperfections cannot reduce spacing more than 50 %.
- Opaque particles trapped within the board cannot reduce the spacing between adjacent conductors to below the minimum spacing specified, or 0.010" whichever is greater.
- The imperfection cannot propagate as the result of testing or processing.

6 Conductor Definition

Surface Mount pad of 25 mil pitch shall be held to within +0.0015"/-0.001" and pads 20 mil pitch and less shall be held within +0.001"/-0.001" of the electronically defined nominal pad width.

External pad breakout is unacceptable. The minimum conductor to land junction interface shall never be less than 0.002".

Layer to Layer registration between all layers shall not exceed a positional tolerance of ± 0.005 ".

7 Copper Plating

Electroless copper shall be used only as a preliminary process to provide a conductive surface for Electro-plated copper. Direct metallization and full build Electroless copper methods are not acceptable without prior written approval from BEI.

Copper plating voids shall meet IPC-6012 Class 3.

Methods used to monitor the copper plating must include micro-sections of the smallest plated hole size and at least one component hole for the specific part number being built

(minimum of 3 holes) from an area of the board having the lowest plating current density. See section 17 Micro-sectioning.

The supplier is required to keep the actual micro-sections for at least one year and be able to provide the micro-section upon request from BEI.

PCB circuitry must conform to IPC - 6012 Class 2 except the minimum average copper thickness in all plated through holes, blind vias, and buried vias shall be 25.4 microns (1.0 mils) with the minimum measurement of at least 20.3 microns (0.8 mils).

The minimum internal annular ring must be 25.4 microns (1 mil) at land / conductor junction, and tangency elsewhere.

The minimum external annular ring must be 50.8 microns (2 mils) at land / conductor junction, and 25.4 microns (1 mil) elsewhere.

8 Surface Finishes

8.1 Electroless Nickel Immersion Gold (ENIG)

Immersion Gold thickness shall be measured at 0.051 to 0.203 um (2 to 8 micro-inches) using XRF.

Electroless Nickel thickness shall measure a minimum of 3.0 um (118 micro-inches) using XRF.

ENIG plating finish to be deposited after solder mask. Full body ENIG processing is not allowed.

XRF results shall be reported in Certificate of Compliance under Section 19 Supplier Deliverables.

8.2 Organic Solderability Preservatives (OSPs)

If not called out on the fabrication drawing, some of the acceptable OSPs include those listed below. Others may be added in the future. Regardless of the chemical used, the responsibility for a solderable surface will be the suppliers.

RoHS Process Capable:

- Entek Plus 106 AX HT by Enthone OMI
- M-Coat by MacDermid
- Gliccoat-SMD F2LX and F2LXPK by Shikoku Chemicals, Inc.

Non RoHS Process Capable:

- Entek Plus 106 AX by Enthone OMI
- Entek Plus 106 AX HT by Enthone OMI
- M-Coat by MacDermid
- Gliccoat-SMD F2LX and F2LXPK by Shikoku Chemicals, Inc.

Surface Finishes shall be sufficient to provide a solderable surface for subsequent assembly. Follow solderability Test C in J-STD-003.

The OSP surface treatment must provide excellent solderability and protection of the bare Copper for at least 6 simulated reflow profiles of 260 deg C peak temperature with ~100 seconds above the liquidus (≥ 217 deg C) temperature.

OSP must not deposit or stain gold surfaces in mixed metal designs.

8.3 Immersion Silver (IAg)

Immersion Silver thickness shall be measured at 0.127 to 0.508 μm (5 to 20 micro-inches) thick using XRF. The preferred range is 0.203 to 0.406 microns (8 to 16 micro-inches).

XRF results shall be reported in Certificate of Compliance under Section 19 Supplier Deliverables.

8.4 Immersion Tin (ISn)

Immersion Tin (Sn) shall be a low stress Tin measured 1 to 2 microns (40 to 80 micro-inches) thick like Ormecon CSN FF-W.

No evidence of Tin Whiskers after 14 weeks of storage.

XRF results shall be reported in Certificate of Compliance under Section 19 Supplier Deliverables.

8.5 SN100CL (Nihon Superior) lead free HASL

Solder coating shall be 1.27 to 7.62 μm (50 to 300 micro-inches) thick.

Composition is nominally 99.3% Sn, 0.6% Cu, and 0.1% other inhibitors and proprietary components. Copper is to be maintained between 0.60% and 0.85%.

Solder thickness is to be measured where applicable by XRF at the geometric center of the pads. If there is a visibly thick area of the deposit, the thickness shall be measured at the thickest part of the solder. Pads selected for measurement must include: pads of the finest pitch (one pad in both the X and Y direction must be measured), pads of the next finest pitch, 50 mil pitch pads, and a capacitor/resistor pad. Measurements must be taken on both sides of the board. Isolated areas may be as low as 40 micro-inches provided that they maintain a solderable surface. The pad must be visually bright and

smooth when viewed at 3X. Results shall be reported in Certificate of Compliance under Section 19 Supplier Deliverables.

8.6 HASL (Tin/Lead) NON RoHS

PCB's with Tin/Lead solder coating shall have an average solder thickness between 0.0001" and 0.001", with no points below 0.00004", and no points above 0.0015". The copper shall be completely covered with no dewetting or nonwetting.

Solder composition shall be between 50-70% tin and form a smooth homogeneous surface.

Solder thickness is to be measured where applicable by XRF at the geometric center of the pads. If there is a visibly thick area of the deposit, the thickness shall be measured at the thickest part of the solder. Pads selected for measurement must include: pads of the finest pitch (one pad in both the X and Y direction must be measured), pads of the next finest pitch, 50 mil pitch pads, and a capacitor/resistor pad. Measurements must be taken on both sides of the board. Isolated areas may be as low as 40 micro-inches provided that they maintain a solderable surface. The pad must be visually bright and smooth when viewed at 3X. See section 19 Supplier Deliverables for reporting of results where applicable.

8.7 Gold Contact Plating

Should the board require selective, hard gold plating for edge fingers, switch contacts, etc. an electrolytic plating process shall be used.

Plate contact features with 0.762 microns (30 micro-inches) minimum of electroplated hard Au over 3.0 microns (118 micro-inches) minimum low stress Ni.

Nickel and Gold plating shall be restricted to the contact areas. There shall be no extraneous, loose or nodular Ni or Au plating on traces or adjacent plated holes.

Bi-Level Gold: Plate contact features with 0.762 microns (30 micro-inches) minimum of electroplated hard Au over 3.0 microns (118 micro-inches) electroplated Ni. The remaining plated features must use one of the two following options:

- Electroplate (Flash) 0.127 - 0.508 microns (5-20 micro-inches) Au on remaining exposed metal surfaces (solder pads).
- Electroless Gold thickness shall be measured at 0.076 to 0.203 um (3 to 8 micro-inches) using XRF.

XRF results shall be reported in Certificate of Compliance per Section 19 Supplier Deliverables.

9 Soldermask

9.1 General

Soldermask shall be in accordance with IPC-SM-840 type photoimageable (LPI) class T.

Soldermask – soldermask over bare copper, green both sides.

Soldermask or soldermask residue on any SMT pad, test via or fiducial is unacceptable. When SMT pads are specified as “soldermask defined”, minimum pad widths must not be violated. This shall not apply to pads which have soldermask intentionally “encroached” onto the pads.

There shall be no missing soldermask on or between conductors.

Unless otherwise stated maximum solder mask clearance and registration must be held within ± 0.003 ".

9.2 Soldermask finishes

Non RoHS compliant PCBs may use soldermask that provides a matte, satin, or semi-gloss finish. Glossy finishes are not allowed.

For RoHS compliant PCBs the soldermask shall provide a matte or satin finish. Glossy or Semi-gloss finishes are not allowed. Solder masks shall consist of any one of the following in no order of preference:

- Huntsman Probimer 65: green, semi-matte finish
- Huntsman Probimer 65 Halogen Free: green, semi-matte finish
- Huntsman Probimer 77: green, matte or semi-matte
- Huntsman Probimer 77 Halogen Free: green, matte or semi-matte
- Enthone Enplate DSR3241 (MD) G: green, matte finish
- Taiyo PSR-4000HFX Satin Halogen Free: dark green, satin finish
- Taiyo PSR-4000MP: dark green, matte and satin finish

For RoHS compliant boards, alternate materials must adhere to the limits for banned materials.

10 Via Plugging

Via plugging and via encroachment is often associated with BGAs. Thermal pads for QFNs, SONs, and Dpaks are also popular applications. Vias should never be plugged from both sides of the PCB. BEI considers the minimum solder mask web to be 6 mils

wide on these packages. If not addressed by customer documentation like CAD layers or fabrication drawing notes, please notify BEI. The data can then be reviewed for proper disposition.

Test point vias must not be plugged.

Plugging must be after the specified surface finish has been applied. Plugging prior to this is unacceptable.

A minimum of 95% of the specified vias must be plugged to allow multiple exposures to vacuum draw down from test equipment. The height of the via plug shall be no more than 0.002" above the soldermask. The via plug material shall not fill more than 50% of the depth of the hole.

For vias that are to be plugged, there shall be openings in the primary solder mask up to 0.006" larger than the diameter of the drill used to make the hole. These openings shall be on both sides of the board. The intent is to have the hole clear of soldermask to prevent entrapment of material during the final surface finish process. However, after plugging, the epoxy must completely cover the pad. No board will have plugs applied by this method to both sides of the same via.

11 Filled and Capped Via

Filled and capped vias as designated in the drill table shall be filled with only non-conductive polymer Peters PP2795 or equivalent. For RoHS compliant boards, alternate materials must adhere to the limits for banned materials.

Fill voiding shall be less than 33% of the entire via.

Filled vias must be planarized and plated over with copper and surface finish on both top and bottom of the PCB.

Reduction of surface copper wrap due to via planarization shall not be greater than 50% of the maximum plated surface copper for that via structure.

Any dimple or recession in the finished plugged and capped via shall be no greater than 0.002".

12 Marking

Unless otherwise specified, All boards shall be marked with the supplier logo, UL Flammability Rating, date code, part number and revision, in etch on the solder (bottom) side of the board. The markings shall be located so that they are visible after assembly. Preferred date code marking shall be week-year (wwyy). It is preferred that a lot code be included on the board for improved traceability.

Silk-screen ink must be non-conductive, color white, unless otherwise specified. There shall be no silk-screen ink on any SMT pad, component or test point pad, or any other metal surface. The supplier is allowed to remove the offending areas on the legend artwork when necessary.

13 Electrical Test and HiPot Test

Unless otherwise specified, all boards shall be tested to IPC-9252, Table 4-1 for designated IPC Class.

The supplier shall perform a net list comparison prior to test fixture development. Any discrepancies must be reported to BEI in writing for review.

All boards shall pass an electrical net list test. Complete 100% test coverage is required, which includes all nets, test points, test point vias, and all pads not covered with soldermask. If net list data is not provided, or is in an unusable format, a net list is to be extracted from the supplied part specific database. However, if net list testing is a specified requirement on any customer specification, or part specific master drawing, BEI must be notified to determine if net list extraction is acceptable.

Test programs shall not be made from a “golden board”.

Hipot testing, when required, will also be performed on 100% of the boards.

Each board that passes electrical test or Hipot test shall be immediately stamped with each stamp using permanent non-conductive ink. Preferred placement of stamp is on the bottom side of the board near the supplier logo and date code. The stamp shall be visible after assembly, and shall not be on any solderable surface, test pad, or fiducial. The stamp is to be on the board, not the panel rails, if possible. If stamping is not possible the supplier shall notify BEI and receive written approval to deviate from this specification. Deviations will be on an individual part basis.

14 Process Capabilities

When tolerances are not specified, the following apply:

Linear Tolerances .XXX = $\pm 0.005"$

.XX = $\pm 0.01"$

Routed board edge to edge tolerance will be $\pm 0.010"$. Overall dimensional tolerance is $\pm 0.005"$ from drilled datum hole to any external profiled (routed) board edge. Internal routed features shall have a tolerance of $\pm 0.005"$ across the feature edges. See Figure 14-1.

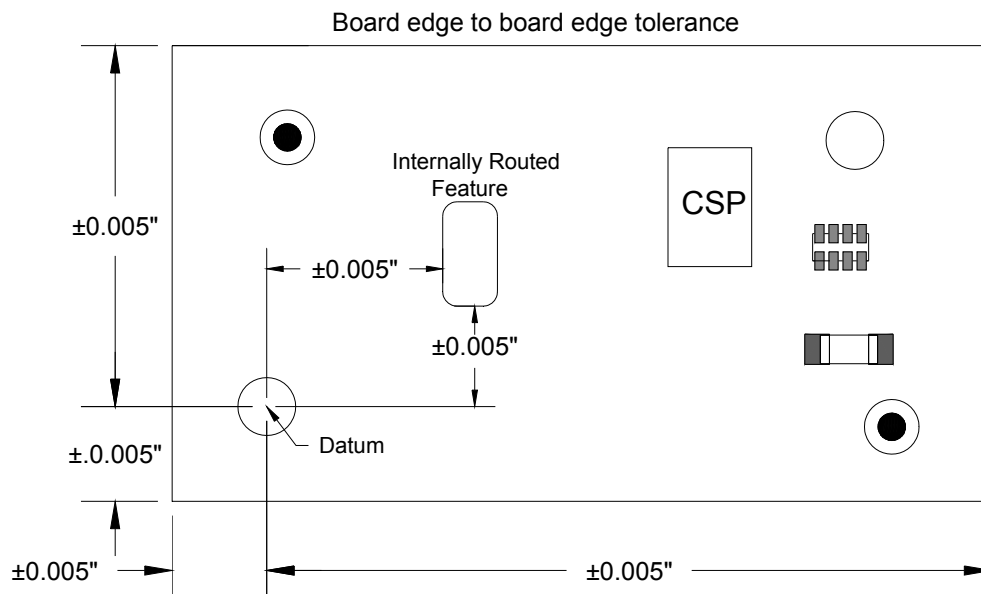


Figure 14-1: Datum to Drill or Edge Feature

Scored board edge to edge tolerance will be $\pm 0.010"$. Overall dimensional tolerance is $\pm 0.005"$ from drilled datum hole to the center of the V-score.

Hole diameters specified for plated holes are to be considered as after plating and any surface finish.

- Finished plated hole diameter tolerance is $\pm 0.003"$.
- Press-fit finished hole size diameter tolerance is $\pm 0.002"$. Several press-fit design standards also dictate drill sizes.
 - GBX from Amphenol TCS: requires a 0.0225" drill and a 0.016" – 0.020" FHS for signal pins.
 - HDM (High Density Metric) from Amphenol TCS: requires a 0.033" drill and a 0.0256" – 0.0315" FHS for signal pins.

- VHDM from Amphenol TCS: requires a 0.026" drill and a 0.020" – 0.024" FHS for signal pins.

Holes > 0.220" may be nibble drilled, or routed and have a tolerance ± 0.005 ".

Non-plated tooling hole diameter tolerance is ± 0.002 ".

Via holes with a finished diameter of 0.020" or less do not have a minimum hole size requirement. However the via holes may not be closed by copper plate.

Hole positioning shall be located within 0.0085" Diameter True Position for all hole locations (± 0.00424 " positional tolerance). See

Figure 14-2.

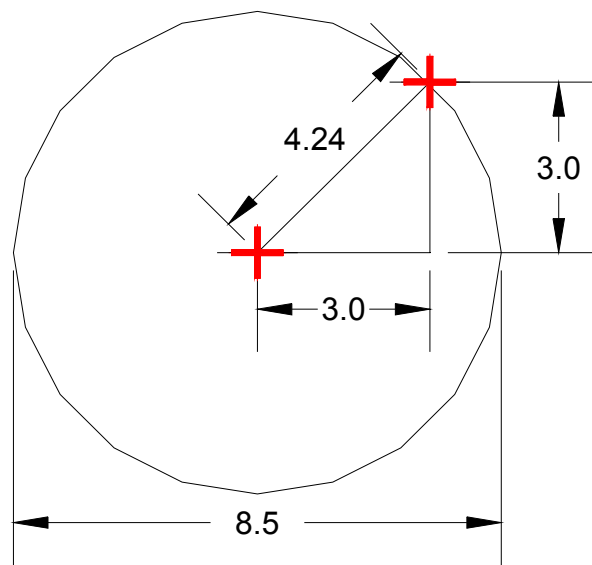


Figure 14-2: DTP Hole to Hole

The Radius True Position is defined as the square root of (delta X squared + delta Y squared).

$$DTP = 2 * RTP$$

Example:

Let's say the center of the hole is located 3 mils right (X) and 3 mils up (Y) from the intended location. So $\sqrt{(3)^2 + (3)^2} = \sqrt{18} = 4.24$ mils = Radius True Position, so the Diameter True Position would be $8.48 \approx 8.5$ mils. The center of the hole must be located within this circle.

Copper feature to copper feature positioning:

- Features spanning < 12" shall be located within 0.006" Diameter True Position (± 0.003 " positional tolerance) of the electronically defined coordinates (cad database or Gerber). See Figure 14-3.

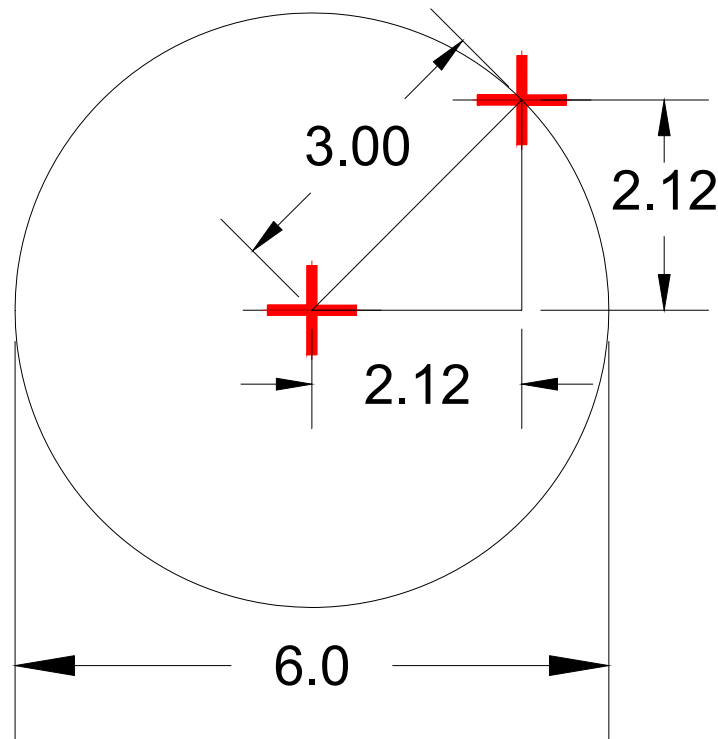


Figure 14-3: DTP Copper Features

- Features spanning > 12" shall be located within 0.0085" Diameter True Position (± 0.00424 " positional tolerance) of the electronically defined coordinates (cad database or Gerber).

15 Repairs

There shall be no repairs to the plated through holes, annular rings, or traces specified as controlled impedance.

Inner layer welds shall not exceed 1 per board per layer when performed prior to lamination. Inner layer repairs, after lamination, are unacceptable.

The maximum length of a repaired trace is 1 inch (2.54 cm) long.

Unless otherwise specified, there shall be a maximum of 1 open circuit repair performed to the external conductors on any board. No more than 10% of any lot may be repaired

for open circuits. Repair per IPC-7721. The repaired area is to be covered with solder mask or epoxy.

Boards with open circuits due to barrel voids, or any other plated-through-hole defect, shall be destroyed.

16 Inspection

All BEI products will have AOI inspection performed on all internal signal layers and a minimum of 10% of the power and ground layers in a production work order.

All BEI products will receive 100% final visual inspection. The minimum magnification shall be a 3X halo light. The first piece from each lot shall be inspected using 10X magnification.

17 Micro-sectioning

Cross-section samples shall include the smallest via hole and at least one component hole.

Cross-sections must be taken such that interconnects in each layer are represented.

Micro-section coupons from the border of the panels will be accepted if they have been proven to be representative of the conditions of the actual finished board.

18 Waiver Requests

For any requested deviations, the PCB supplier shall document the issue and include a proposed resolution. The waiver request should also state whether the job has been put on hold for resolution.

Note: The job can continue to run for any deviations that affect the back-end of the process only.

Waiver requests shall be emailed to the SCA or purchasing agent listed on the Purchase Order. The standard BEI email address is <firstname.lastname@bench.com> however there are exceptions.

The PCB supplier may request a product waiver for issues that are routinely flagged. Once a product waiver is approved by BEI, the PCB supplier is not required to seek BEI approval for any future builds of that same part number revision.

19 Supplier Deliverables

A Certificate of Compliance (C of C) shall be provided with each shipment. The C of C must include:

- Supplier name and division
- BEI part number and revision
- Date codes including quantity of each.
- Signature of authorizing person.
- Date
- Purchase order number
- A statement of RoHS compliance (Material Declaration for RoHS boards)
- Laminate manufacturer and manufacturer part number

Note: A supplier shall be able to show traceability to laminate lot codes.

Each manufacturing date code shall be accompanied by a solder sample. This sample shall be clearly identified, contained in a separate minimum protective package, and included in the shipping container. The container with the solder sample should be clearly marked and labeled as containing "solder sample." The solder sample PCB must be clearly marked on both sides in a permanent fashion in a contrasting color by marker or label.

- For RoHS compliant assemblies, two to four solder samples are required for each batch lot shipped, unless different quantities are indicated by Benchmark staff.
- For non-RoHS assemblies, one to two solder samples are required for each batch lot shipped, unless different quantities are indicated by Benchmark staff.

A First Article Report of all drawing dimensions and print requirements for first delivery of any new part number or revision is required. The supplier shall provide a copy of the report which must include:

- Actual dimensional data
- Tolerances
- Pass or fail statement
- Copy of print with associated reference points to the first article report, i.e. measurement 1, measurement 2 = M1, M2.

-
- Controlled impedance reports where applicable per date code.

Cleanliness testing shall be performed in accordance with IPC-TM-650 Section 2.3.25.

- The bath temperature of 80 degrees C shall be used. Using an alternate or ambient temperature of 22 degrees C would not be acceptable for our Certificate of Compliance.
- The ionic contamination must meet or be below 1.00ug/sq. cm (6.45 ug/sq. inch) of NaCl equivalents when tested with an Omegameter. Certificate of test, that includes test readings, shall be included with each shipment.

Where applicable a micro-section analysis report detailing the findings of the micro-section for each new date code along with the sections are required to be included with the shipment. This report shall include:

- Photo of micro-section
- Average and minimum copper plating thickness
- Dielectric thickness (where required)
- Overall plating quality and integrity

X-Ray Fluorescence (XRF) report prepared based on data taken in section 8 shall be provided for all non-OSP alternative surface finishes including: ENIG, silver, tin, HASL, SN100CL, flash gold and contact gold surface features.

An electrical test certification for every date code with the following information:

- Quantity tested
- Quantity accepted
- First pass yield percentage

When the above deliverables list can not be met the supplier shall contact BEI to request a waiver. If approved, all waivers will be valid for only the issuing BEI Division.

Supplier deliverables will be maintained by Incoming Inspection and will have the same retention time as the inspection history.

20 Handling and Shipping Requirements

20.1 Moisture sensitivity

The fabricator must follow moisture sensitivity guidelines for handling all lead-free capable laminates including:

- Storage of material
- Handling of material during processing
- Baking material after each wet process regardless of processing method
- Packaging of materials

BEI may audit our fabricators to ensure moisture sensitivity procedures are in place and followed.

PCB fabricators must be able to demonstrate that their material suppliers adhere to J-STD-20 and J-STD-33 for material storage, handling, processing and shipping.

When the PCB notes state to “package in moisture barrier bags,” as in RoHS compliant PCBs, the following conditions shall apply:

- PCBs shall be packaged in moisture barrier bags.
- Prior to sealing, bags shall be vacated. It is preferred to purge any remaining air with nitrogen, if available.
- Moisture barrier bags shall contain one Unit of desiccant per 200 square inches of exposed surface area and a humidity indicator card.
 - Desiccant material shall be dustless, non-corrosive, and sulfur free.
 - Indicator cards shall cover 10-30%, or 10-50%.
 - Boards indicating moisture exposure of 20% or greater will be returned.

20.2 Packaging

Printed Circuit Boards shall be packaged to prevent damage and surface scratching.

The supplier's minimum protective package shall assure no loss of solderability to meet expected shelf life based on board finish.

- 1 year shelf life: ENIG, Flash Gold, SN100CL (LF HASL), and PB HASL
- 6 month shelf life: OSP, Immersion Silver, and Immersion Tin

Unless noted otherwise in the PCB notes, supplier may use their standard preferred packaging. PCBs with Silver finish shall be handled per IPC 4553.

Only boards of the same date or lot code may be sealed in the same bundle. Date/lot code and RoHS compliance labels shall be located on the outside of each bundle. The date or lot codes of all of the boards contained in each box shall be printed on the outside of that box.

All shipping containers shall be clearly labeled with PCB part number, date code or lot number, PO number, and quantity. Any shipping carton containing the C of C, solder sample, or X-outs, should be clearly labeled to identify enclosed items.

All packing materials shall be non-static generating (the box to ship the order is exempt from this requirement). Packing "peanuts" of any type, shall not be used.

Shipping container shall not exceed 40 lbs (18.2 kg).

Date/lot code and RoHS compliance labels shall be located on the outside of each bundle.