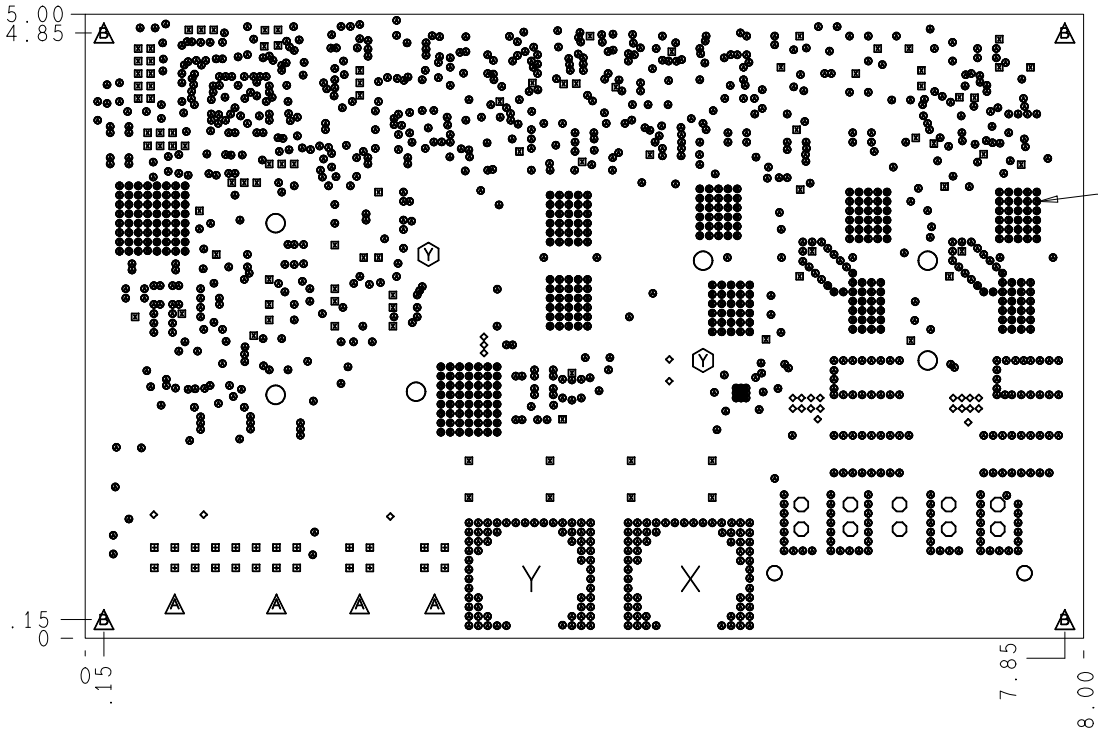


D

C

B

A



14

3		2		1	
REV	CHANGE NOTICE NO.	REVISIONS			
		DESCRIPTION		CHANGED BY	DATE
004	-	ORCAD TO ALLEGRO CONVERSION		LPL	04/26/12
005	-	ADDED VOID AROUND GND VIAS FOR R211, R111 AND R144.		DJG	09/26/12
006	-	ADDED COMPONENTS C174, C175, R249 AND R250.		DJG	10/17/12
-	-	-		-	-
-	-	-		-	-

FABRICATION NOTES:

- 1.) MATERIAL SELECTION:
370HR OR EQUIVALENT UL RECOGNIZED ZPMV2 MIN. 130C FLAME CLASS V-0 OR BETTER, MINIMUM CTI RATING OF 175, .062 +/- 0.007 THICK. MATERIAL PER IPC-4101
SOLDERABLE SURFACES TO BE ENIG (ELECTROLESS NICKEL IMMERSION GOLD) FINISH.
ALL LAYERS TO BE 2 OZ COPPER FINAL MINIMUM THICKNESS
- 2.) SOLDER RESIST: THE USE OF SOLDER RESIST COATING SHALL BE IN ACCORDANCE WITH THE REQUIREMENTS OF IPC-SM-840. ALL SOLDERABLE SURFACES ARE TO BE FREE OF SOLDER RESIST. COLOR- GREEN. USE LIQUID PHOTOIMAGEABLE RESIST.
- 3.) SILKSCREEN: USE WHITE NON-CONDUCTIVE INK. ALL COMPONENT AND TESTPOINT LANDS ARE TO BE FREE OF INK.
- 4.) MANUFACTURER'S IDENTIFICATION: ADD IN ETCH OR TO SILKSCREEN.
- 5.) ELECTRICAL BARE BOARD TEST REQUIRED.
- 6.) DRILL SIZES ARE FINISHED SIZE AFTER PLATING.
- 7.) FABRICATE TO MEET EU RoHS DIRECTIVE.
- 8.) PCB MUST HAVE UL 94V-0 AND CTI RATINGS MARKED ON ONE SIDE.
- 9.) MAX WARP AND TWIST NOT TO EXCEED 0.010 PER LINEAR INCH.
- 10.) MIN. ANNULAR RING: 0.003. MIN PLATED HOLE WALL THICKNESS .001.
- 11.) DIMENSION TOL: XX +/-0.010 : XXX +/-0.005.
- 12.) FABRICATE IN ACCORDANCE WITH IPC-600 OR IPC-6012 LATEST REVISION CLASS 2.
- 13.) COPPER THIEVING OF THE SIGNAL LAYERS IS ALLOWED, SPACING TO ANY EXISTING BOARD FEATURE TO BE 0.060 MINIMUM.
- 14.) ALL (365) 12.1 DIAMETER HOLES TO BE PLUGGED FROM THE TOP SIDE (COMPONENT SIDE) WITH EITHER UV OR THERMALLY CURED PLUGGING MATERIAL. THE PLUGGING MATERIAL SHOULD NOT DRIP OUT THE BOTTOM SIDE OF THE PCB... PER BENCHMARK DOCUMENT BE-46003 NOTE 10.

DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
•	12.0	+3.0/-3.0	PLATED	966
•	12.1	+3.0/-3.0	PLATED	365
◊	35.0	+3.0/-3.0	PLATED	26
■	40.0	+3.0/-3.0	PLATED	96
■	55.0	+3.0/-3.0	PLATED	24
○	110.0	+3.0/-3.0	PLATED	10
○	118.0	+3.0/-3.0	PLATED	2
X	222.0	+3.0/-3.0	PLATED	1
Y	261.0	+3.0/-3.0	PLATED	1
○	150.0	+3.0/-3.0	NON-PLATED	6
△	152.0	+3.0/-3.0	NON-PLATED	4
△	156.0	+3.0/-3.0	NON-PLATED	4
⊙	187.0	+3.0/-3.0	NON-PLATED	2

ALL DIMENSIONS ARE IN INCHES [MILLIMETERS] UNLESS OTHERWISE SPECIFIED.

TOLERANCES UNLESS OTHERWISE SPECIFIED

1 PLACE: ± 0.020 IN [0.500 MM]

2 PLACE: ± 0.010 IN [0.250 MM]

3 PLACE: ± 0.005 IN [0.127 MM]

ANGLES: ± 1.0°

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Benchmark Electronics

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THIRD ANGLE PROJECTION

DRAWN BY: PL LEE

DATE: 24Oct2012

DESIGN LOCATION:

ARCHIVE LOCATION:

TITLE:

RAW PCB, TENNANT - SCRUB (MAIN)

MATERIAL: SEE NOTES

FINISH: SEE NOTES

SCALE: 1:1 & NOTED

SHEET 1 of 1

SIZE C

USED ON OR PRODUCT IDENTIFIER: For Assembly PN is 1200744

FAB SCHEMATIC PN

DRAWING NUMBER: Q25038

CAGE NUMBER: 39887

REV: 006

1 ALLEGRO